Intelligence Will Be Everywhere

MIPS by GF overview

September 2026

GlobalFoundries at a Glance

$6.79B
2025 revenue

2.3M
2025 wafer shipments (300mm eq.)

500+
customers

4
manufacturing sites across three continents

~13,000
employees

~9,000
patents

GF Business Teams

Tim Breen
Chief Executive Officer

Ed Kaste
SVP, CMOS business

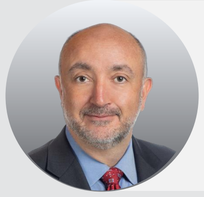
Sameer Wasson
SVP & CEO of MIPS, by GF

Téa Williams
SVP, Silicon Photonics & RF business

Kannan Soundarapandian
SVP, Power business

MIPS : ARC by GF

Physical AI is built on MIPS

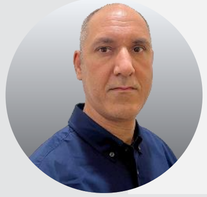


Yankin Tanurhan
Chief Technology Officer, MIPS

Drew Barbier
Atlas Processor Platforms business

Manav Mediratta
ASSP & custom solutions business

Sam Grove
Atlas Software Tools business



Manoj Koul
Physical AI business

Michael Zirngibl
WW Business Development

Anubha Tewari
Strategy & Operations

James Prior
MIPS Marketing

Global Scale & Depth of IP, Silicon & Software

MIPS + ARC BY GF

41
AI, MPU, MCU & DSP cores

300+
customers

200M+
ADAS SoCs shipped

1st
RISC-V company at scale

2nd
Largest IP provider

750+
engineers

GLOBAL FOOTPRINT FOR R&D, SUPPORT & SALES

Americas

Asia

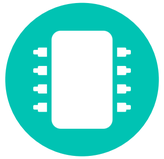
Europe

MIPS : ARC by GF

MORE THAN IP

Platform Strategy

MIPS delivers the whole stack: Open, standards based AI & compute IP, ASSP and custom solutions at worldwide scale

Compute	Subsystems	Platforms	Middleware	Ecosystem	Worldwide Scale
					
AI & RISC-V processor core IP	Analog & physical	Reference ASSPs on GF automotive nodes	RTOS, AUTOSAR & software stacks	Vector · Green Hills · debug & trace	Global R&D, support & manufacturing

PROVEN IP + PRODUCTION SILICON + A SOFTWARE ECOSYSTEM THE INDUSTRY ALREADY TRUSTS

MIPS ARC by GF

RISC-V is Now Mainstream

Open, standards-based RISC-V processors have crossed into volume

Safety-certified

ASIL-B/D, ISO 26262 production-grade, not a science project

Shipping at Volume

200M+ ADAS SoCs already in the field with same micro-architecture

Software-first

Take control of your roadmap — off-the-shelf is someone else's vision

Open and Growing

RISC-V profiles + a maturing ecosystem; automotive ~37% CAGR

MIPS Product Lines

MIPS Platforms

Atlas Processor Platforms

Enabling Physical AI with scalable processor IP for mission critical platforms that require safety and low-latency event processing

MIPS Atlas portfolio of scalable IP based on open RISC-V ISA

- 64-bit Embedded applications processors
- 32-bit High-performance microcontrollers
- Optimized for customer Physical AI workloads

ASSP & Custom Solutions (ACS)

Delivering custom silicon optimized for Physical AI platforms using scalable, standards-based technology

- Optimized SoC architecture design
- Platform implementation optimization for SWaP-C
- Mixed-signal, analog and power
- Safety capable, auto and industrial qualified

Atlas Software & Tools

Enabling modern platform design with virtual platforms to evaluate IP and shift-left software/hardware co-design

- MIPS Atlas Explorer virtual platform for earlier insights and smarter designs
- ASIP tools for custom processor cores tailored to workloads with full software support
- Code optimization and migration services for ease of adoption and efficiency

Physical AI

Full Platform solutions that simplifyPphysical AI adoption

- Application Specific IP–AI cores, mixed signal technology and more
- Integration of industry standard protocols
- Solutions integrating customer IP and third-party IP
- MIPS ForgeSTAC reference enablement platforms

Compute for Automotive, Industrial, IoT & Comms

Compute Tier Cores	Automotive	Robotics	IoT	Communications
AI Acceleration S8200 · NPX6	Perception offload	Manipulation & vision AI	On-device TinyML	AI-in-network / RIC
64-bit Application / Host MPU P8700 · RPX-100 “A720”-Class MPU	ADAS & cockpit	Autonomy & perception	Edge AI gateway	Edge gateway / CPE
Real-Time Linux MPU I8500	Zonal gateway	Robot controller	Industrial edge	Packet processing
High-Performance / Safety MCU M8500 · RHX-100 · RMX-500	Motor & brake control	Motion & servo	Industrial node	Line-card control
Entry MCU RMX-100	Smart sensor / actuator	Safety co-processor	Low-power endpoint	Management MCU
Digital Signal Processing VPX	Radar / lidar / audio	Vision & sensor DSP	Voice & audio	Baseband / modem

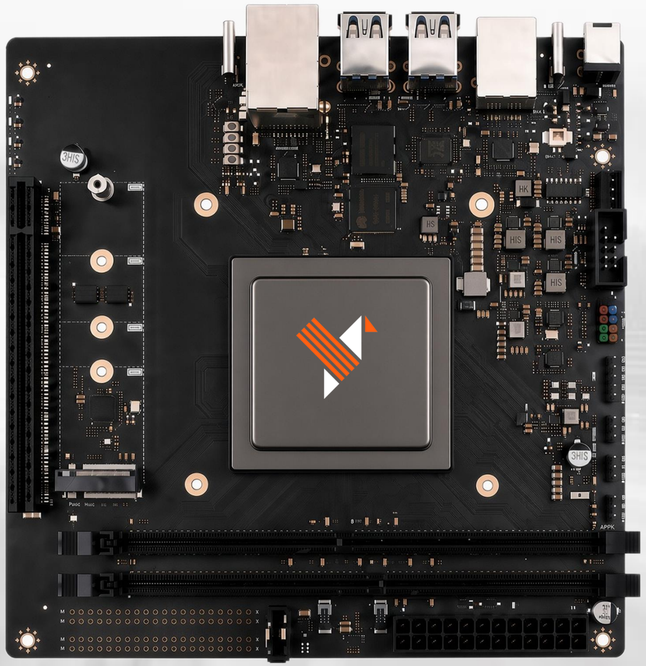
MIPS : ARC by GF

MIPS Reference Platforms

Acies

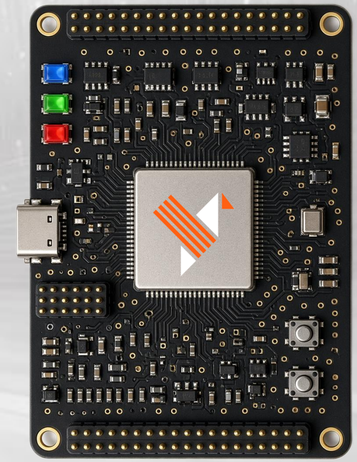
Inference-native AI

Aegis



Safety-native CPU

Actus

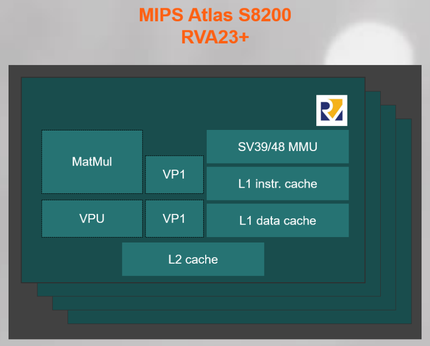


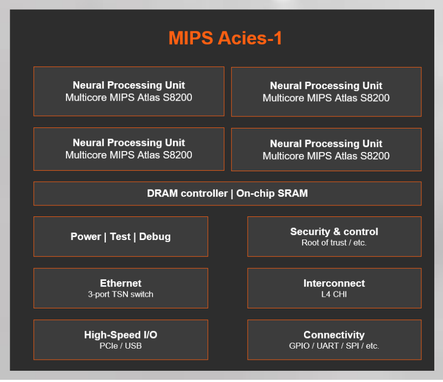
Event-native MCU

MIPS Acies-1: Inference-native AI

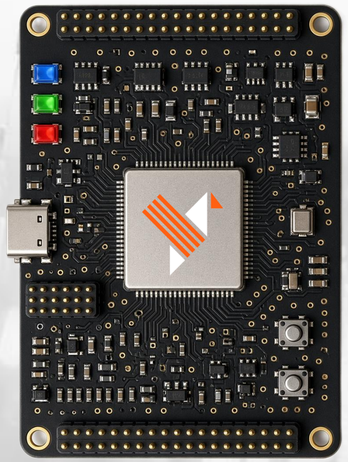
Acies: keen edge; rapid; perception

- Acies-1 is an edge accelerator for modern AI
  - Native agentic capabilities for robotics and automation devices
- Standards-based: MIPS Atlas S8200
  - RVA23 profile with RVV and VME
- Llama.cpp and Qwen for LLMs, plus vision transformers (ViTs) and Vision-Language-Action models
- Atlas SDK and Graph Performance Simulator, with IREE-based MLIR for TensorFlow, PyTorch and ONNX
- Easy-to-integrate M.2 PCIe form factor



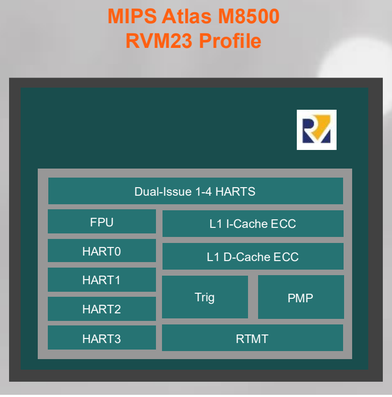


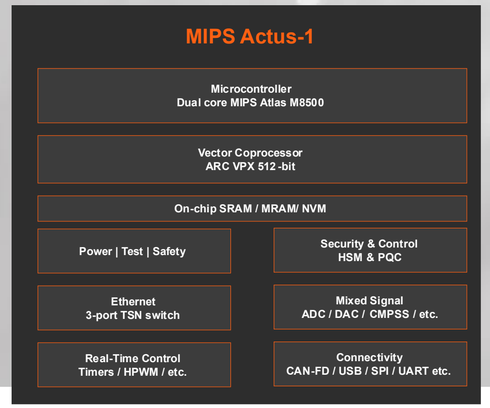
MIPS Actus-1: Event-native MCU



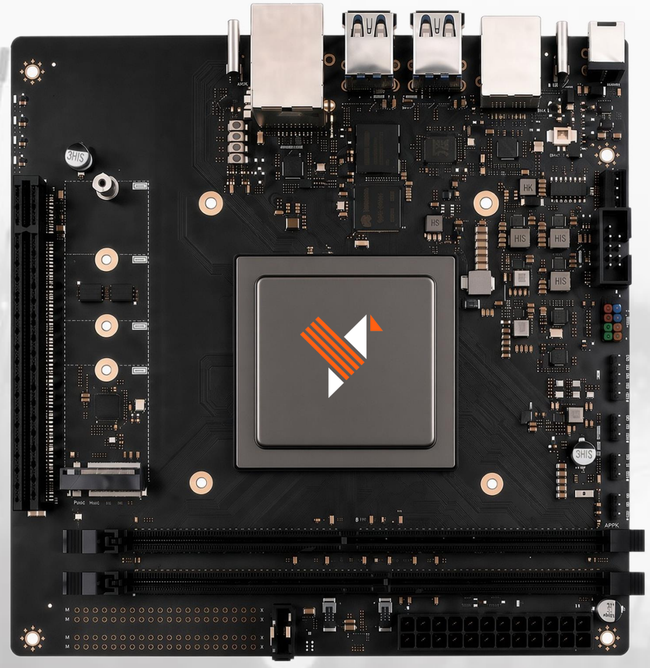
Actus: drive; urge; impetus; action

- Actus-1 is a real-time developer platform
  - Enabling event-driven embedded applications:
    - motion control; sensor fusion; predictive maintenance
- Embedded Intelligence
  - MIPS Atlas M8500: RMV23 profile support
  - Real-time multithreading architecture with FoC acceleration
  - ARC VPX 512-bit vector co-processor
- Single-board computer form-factor for easy integration and lab use
- Standards Based Development
  - ISO 26262 & ISO 21434



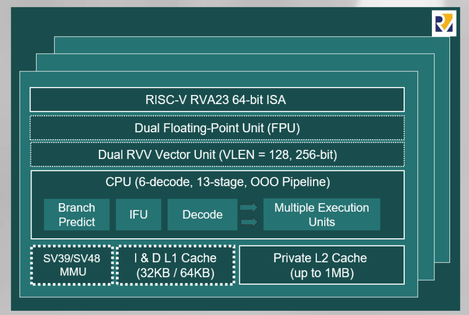


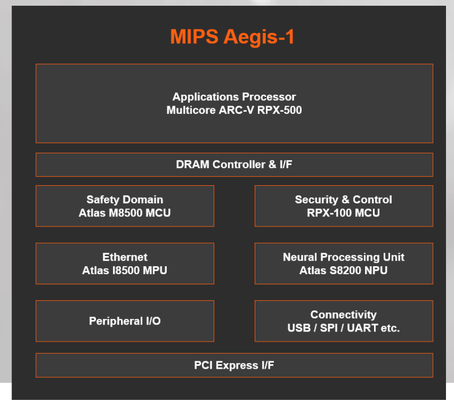
MIPS Aegis-1: Safety-native CPU



Aegis: the shield; protection; safety; guidance

- Aegis-1 is a RISC-V applications developer platform
  - Enabling RISC-V Android & Linux development
  - Accessible to open source & commercial ecosystem
  - Develop mission-critical platforms
  - Enabling agentic workloads outside the data center
- Clean-sheet design, built from ground up for safety
  - Fastest licensable safe CPU IP
- Single-board computer form-factor for easy integration and lab use
- Standards Based Development
  - ISO 26262 & ISO 21434





Earlier Insights | Smarter Designs

Translating Workloads into Platforms

Atlas Explorer Virtual Platform
for Atlas IP Core Models

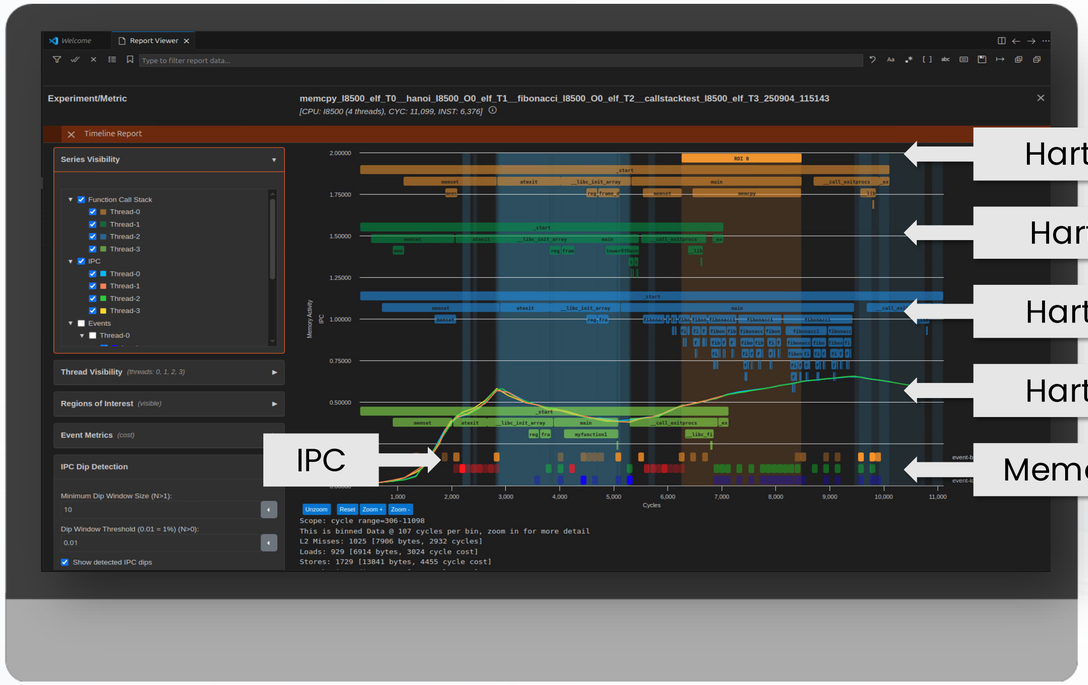
Shift-left Development

Start software optimization before,
silicon, FPGA, or RTL availability

Platform Design Insights

Branch trends, load/store activity, ALU usage,
register pressure, cache locality, IPC & more

MIPS Atlas Explorer
for Visual Studio Code



MIPS Ecosystem for Software

Green Hills SOFTWARE INC

+

MIPS : ARC by GF

for

Safety Certified MCU Platforms

Model Zoo for AI

PyTorch

TensorFlow Lite

Model Lowering & Platform Optimization

Atlas Access Program

60+

Members Worldwide

Customer Highlight: FPGA to ASIC

apex compute

What has stood out throughout our engagement with MIPS is how seamlessly the teams worked together to accelerate innovation.

By combining Apex's design expertise with MIPS' deep implementation capabilities and close alignment with GlobalFoundries, we created a highly collaborative development model that allowed us to move quickly, solve challenges in real time, and streamline the path from FPGA to ASIC.

Hasan Unlu
Founder and CEO of Apex Compute

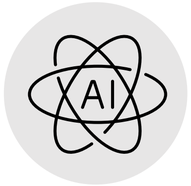
MIPS : ARC by GF

Physical AI is Built on MIPS

Software to Silicon with RISC-V

Software-first processor IP design

Modular workload extensions



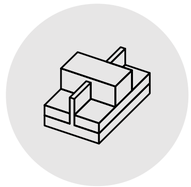
Processor IP optimized for physical AI

Open standard instruction set architecture

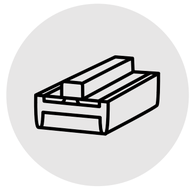
Architecture Influences Technology

Technology Enables Architecture

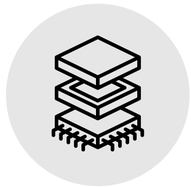
Optimized Technologies



World's most feature-rich FinFET



FDX: Lowest power, highest integration



Advanced packaging: size, power, performance

Multi Purpose Intelligence

Atlas Portfolio of RISC-V Processor IP

- Optimized for Sense, Think, Act, Communicate

Microarchitecture optimizations for efficiency in ultra-low power process technology

Software-first Design

Atlas Explorer Virtual Platform

- Core Models of Atlas IP & subsystems

Silicon Proven

200M+ ADAS/AV SoCs Shipped

- 50+ Global Auto OEMs / 1200 Car Models

RISC-V at Foundry Scale

ASSPs Optimized for Size, Weight, Power, Cost

Dedicated I/O devices enabling dense SoC integration

Industry leading integrated RF & embedded memory

Physical AI is built on MIPS

Scale & heritage

#1 RISC-V IP portfolio

#2 processor IP provider

3.5B+ units shipped annually

200M+ ADAS SoCs deployed

40+ years of innovation

25+ years of software tools expertise

450+ patent assets

Market position

Over 500 customer engagements including:

9 of top 12 automakers

8 of top 10 aerospace and defense primes

13 of top 15 AI and data center infrastructure silicon suppliers

5 of 5 leading robotics and industrial automation vendors

Holistic capability

Single portfolio of AI, IP, software tools and custom solutions

Leading open standards definition and development

Focus on efficiency for Physical AI

Worldwide R&D and support

MIPS ARC by GF

Physical AI is built on MIPS

MIPS.com

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