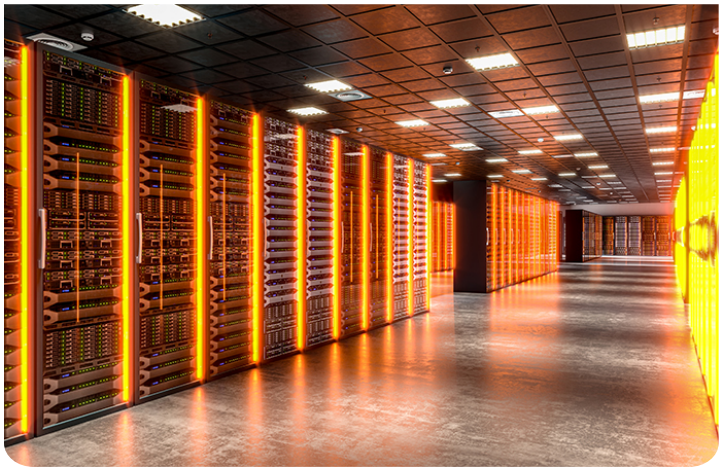
PRODUCT BRIEF

MIPS Atlas I8500

The MIPS **Atlas I8500** processor provides industry-leading throughput and real-time processing for dataplane, embedded edge and communications markets.



Features

- Energy efficient 64-bit RISC-V application processor
- RVB23 compliant
- 4-Way Simultaneous Multi-Threading (SMT)
- Hardware-assisted hypervisor and security
- Tightly-coupled accelerator interfaces
- Supports Linux and RTOS based applications
- Area-and power-optimized design

Efficient Throughput

Data movement intensive applications require immediate, low latency processing with predictable and secure data orchestration. These workloads are typically highly parallel and composed of multiple data streams or packetized tasks.

The MIPS I8500 is designed to meet these requirements for AI driven workloads, efficiently offloading data management for dataplane and communication systems while delivering high performance real time processing for edge and embedded applications.

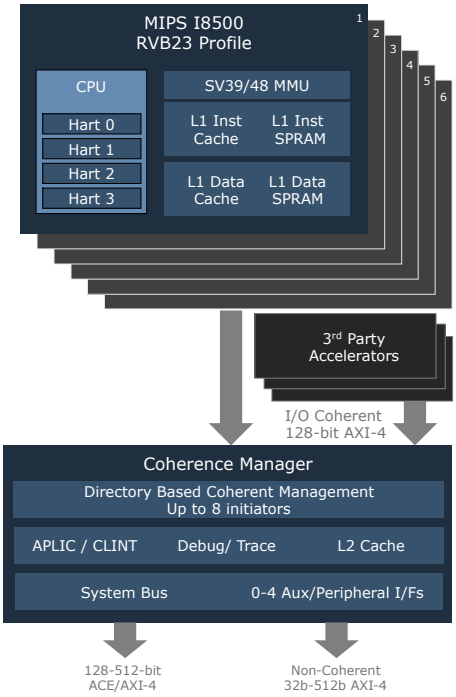
The MIPS I8500 is the first RISC-V processor to support 4-way Simultaneous Multi-Threading (SMT), providing highly parallel execution and zero latency context switching. It is a fully-featured 64-bit CPU built on the RISC-V RVB23 ISA that also incorporates performance-enhancing MIPS-defined instructions. Together, these capabilities deliver a best in class solution for efficient data management and real time processing.

The 9-stage in-order pipeline combined with up to 4-way SMT provides a very efficient, high-throughput solution that can be used with as few as 1 or 2 cores, while being scalable up to 6 cores and 24 threads per cluster.

The MIPS I8500 cores can be configured to meet different application requirements with options for Level 1 (L1) cache sizes, and support for 1, 2, or 4 hardware threads.

The I8500 Coherence Manager maintains Level 2 (L2) cache and system level-coherency across all cores, main memory, and I/O devices. The I8500 is a configurable and synthesizable solution: the clusters can be configured with a variable number of cores, I/O coherent interfaces, and L2 cache size up to 2MB.

The I8500 Coherence Manager has an AMBA® ACE interface that enables the processor's multiprocessing system to coherently scale up to many heterogeneous clusters at the system-on-chip (SoC) level. Each cluster supports up to 6x I8500 cores, each with up to four hardware threads per core or heterogeneous clusters comprising CPU and other accelerators at the system-on-chip level.



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Simultaneous Multi-Threading

The MIPS I8500 supports up to four simultaneous hardware threads (four harts in RISC-V terminology) running on a single CPU instance. Its superscalar, triple issue design allows multiple instructions from multiple harts to execute each cycle, with zero overhead context switching.

Scalable Multi-Cluster Architecture

Building upon SMT at the core level, the I8500 scales efficiently through multi core clusters (up to six cores) and multi cluster SoC implementations, enabling large numbers of parallel execution threads.

Heterogenous Compute

The Coherence Manager enables heterogeneous compute clusters with shared, coherent caches and system interfaces, supporting a mix of CPUs, integrated I/O, and accelerators. It also provides options for tightly coupled L1 RAM or streaming engine buffers.

Deterministic Execution

The short, in-order pipeline with zero overhead context switching and addressable level-1 RAM offers deterministic and real-time processing and low-latency access to memory and peripherals.

Hardware Virtualization

The MIPS I8500 provides hardware-assisted virtualization based on the RISC-V H-extension to safely and securely consolidate multiple virtualized environments within a single core. It can dynamically and deterministically allocate CPU bandwidth per application.

Security and Reliability

The MIPS I8500 implements the RISC-V Physical Memory Protection (PMP) architecture with 16 regions, enabling isolation of critical assets from potential hazards.

I/O Coherence Units (IOCUs)

Hardware I/O coherence is provided by the I/O Coherence Unit (IOCU), which maintains I/O coherence of the caches in all coherent CPUs in the cluster. Up to eight IOCUs (total number of cores + IOCUs must be no greater than eight).

Cluster Power Controller (CPC)

The Cluster Power Controller (CPC) allows individual CPUs within a cluster to have their clock, power, or both gated off when idle. It manages the shutdown and ramp up sequences for all cores and can be controlled via software (through registers) or hardware (through a signaling interface).

Interrupt Controller

The I8500 interrupt architecture includes the Advanced Platform-Level Interrupt Controller (APLIC), Advanced Core Local interrupt (ACLINT) Machine-level Timer, ACLINT Machine-level Software Interrupt (MSWI), ACLINT Supervisor-level Software Interrupt (SSWI) and a Watchdog Timer (WDT). The APLIC Interrupt Controller handles the distribution of interrupts among the CPUs and harts in the cluster.

Global Configuration Registers (GCR)

The Global Configuration Registers (GCR) are a set of memory-mapped registers that are used to configure and control various aspects of the Coherence Manager and the coherence scheme.

Custom GCRs

The Coherence Manager provides up to 64 KB of custom registers for system level control. Users define these registers and instantiate them into the design. Two global registers—Global Custom Base and Global Custom Status—are supplied by the Coherence Manager.

Debug Unit

The Debug Unit (DBU) enables debug using a probe connected through a JTAG scan chain. The DBU contains the single TAP controller in the cluster, which can access registers through the cluster. The DBU also contains a RAM to hold instructions and data accessed by the cores while in debug mode. The debug port supports multi-core debug via the JTAG interfaces.

Trace Funnel

The I8500 core includes RISC-V compliant N-trace support for real-time tracing of instructions, data addresses, data values, and performance counters.

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