

ARC Sensor and Control IP Subsystem

Highlights

- Integrated, pre-verified hardware and software IP subsystem
- ARC EM processors with cache and DSP extensions deliver extremely low gate count and highly efficient processing performance
- Extensive library of software DSP functions enable sensor signal processing
- Hardware accelerators boost performance efficiency and reduce power consumption by up to 85%
- Digital and analog interfaces provide multiple input and output options for sensors and actuators

Target Applications

- Industrial
 - Real-time control
 - Robotics
- Automotive
 - In-vehicle networking
 - ABS
 - Electric power steering
 - Digital motor control
- Consumer
 - Mobile phones/tablets
 - E-metering
 - Home automation
 - Connected appliances
- Portable Medical Devices
 - Blood-pressure monitors
 - Heart-rate monitors
 - Digital thermometers

Overview

The DesignWare® ARC® Sensor and Control IP Subsystem is a complete, pre-verified, hardware and software solution optimized for a wide range of ultra-low power embedded sensor and general embedded control applications. It is designed for fast and easy integration within a larger system context. The subsystem is either the basis of an independent system controller on a system-on-chip (SoC) or it provides higher abstraction to a main controller by combining sensor inputs. The fully configurable ARC Sensor and Control IP Subsystem includes the choice of a low gate count and energy-efficient ARC EM4 or EM6 processor for control processing, accompanied by an extensive collection of I/O functions and DSP accelerators. The software libraries of the subsystem contain small footprint drivers for all I/O, plus DSP functions supporting signal processing. The integrated solution is optimized for small area and low power.

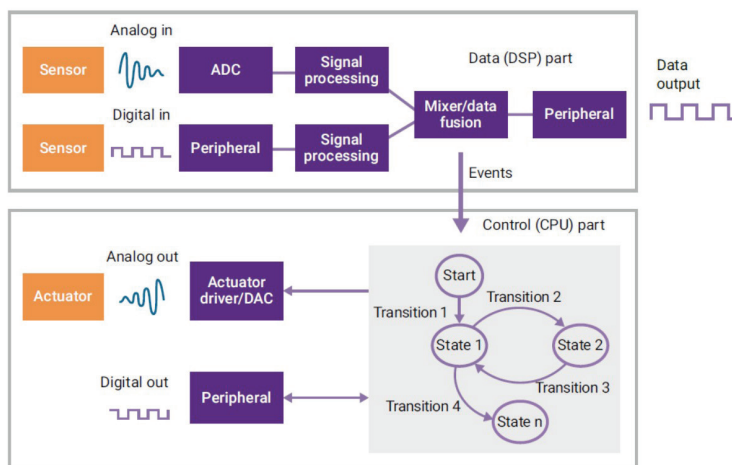


Figure 1: ARC Sensor and Control IP Subsystem functional block diagram

The ARC Sensor and Control IP Subsystem supports multiple integration approaches for sensor interfaces:

- **PCB level integration:** sensor is contained in a different package from the package that contains the subsystem
- **System-in-Package (SiP):** sensor and subsystem are integrated as a SiP but each on a separate die
- **Single-Die:** both sensor and sensor subsystem are part of the same die

The MIPS ARCHitect IP configuration tool allows users to fully configure the subsystem. Configuration options include processor settings, number of digital and analog I/O interfaces and use of hardware accelerators. The ARC MetaWare Development Toolkit can be used for development of user applications that are built upon the Sensor and Control IP Subsystem software libraries.

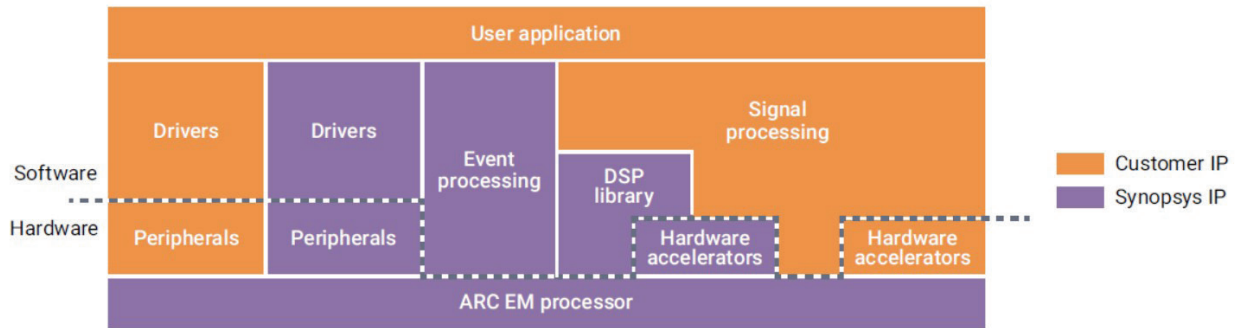


Figure 2: ARC Sensor and Control IP Subsystem system view

Software Architecture

The ARC Sensor and Control IP Subsystem software offering includes a library of DSP functions for signal processing such as linearization, filtering, complex math, matrix/vector and decimation/interpolation. Software drivers are also included to ease I/O peripheral integration.

In lieu of an operating system, a lightweight event processing framework is included with the example implementations to quickly get customers started with subsystem integration.

Hardware Architecture

The Sensor and Control IP Subsystem provides an optimized hardware architecture consisting of an ARC EM4 or EM6 processor, tightly coupled digital I/O interfaces via custom registers and a selection of DSP accelerators.

The software DSP functions provide configuration options to make use of these hardware accelerators. The overall system is highly configurable and extensible (Figure 3).

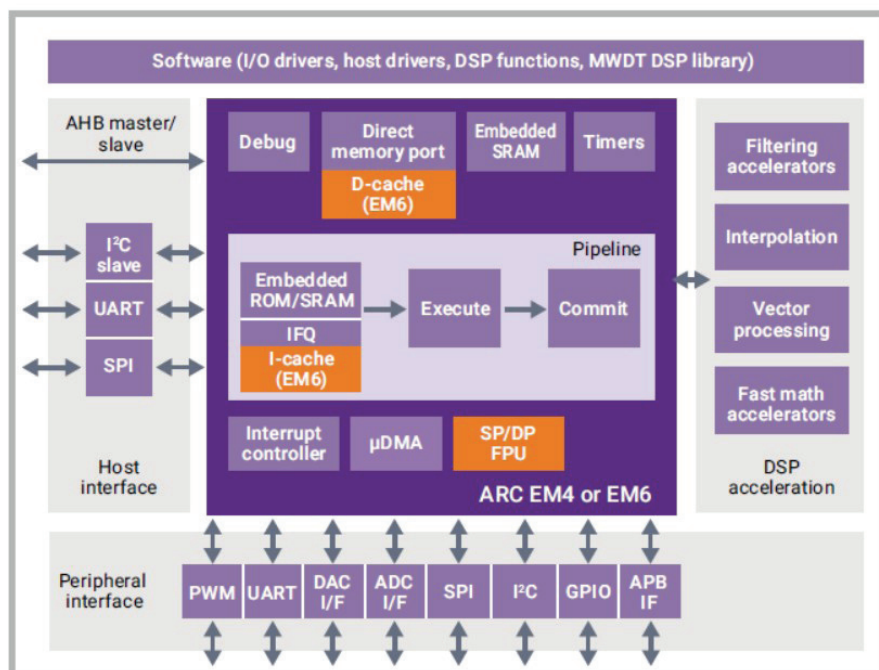


Figure 3: ARC Sensor and Control IP Subsystem hardware architecture

Key Features

- Efficient processor
- Sensor and actuator interfaces
- SoC host and peripheral interfaces
- Hardware accelerators
- Power management
- Software I/O drivers and DSP libraries
- Implementation example
- Demonstrator
- MIPS ARChitect IP configuration tool
- Extension options

Efficient Processing

A power-efficient, low gate count ARC EM4 or EM6 processor is at the center of the Sensor and Control IP Subsystem. Both processor core options support up to 2 MB of closely coupled memory (CCM) for both instruction and data, while the EM6 also incorporates up to 32 KB of instruction and data cache for maximum system performance and flexibility. The EM processors are highly configurable and can be optimized for area and performance using a wide range of parameters.

An integrated μ DMA controller provides cycle-efficient DMA transfers with low gate count and low power consumption. The μ DMA engine supports up to 16 independent channels, and multiple peripheral / memory transfer modes, allowing alternate bus masters to access closely coupled memory (CCM) and subsystem peripherals while the EM processor is in one of its low-power sleep modes.

Users can add or remove features that improve the efficiency of the core for their application. This includes options such as instruction and data closely-coupled memory configurations, instruction and data caches, IEEE-compliant single precision/double precision floating point unit (FPU), address bus width, timers, interrupts, register file structure and debug interface.

Users also have the option of adding custom instructions using the ARC Processor EXTension (APEX) interface.

Sensor Interface

The ARC Sensor and Control IP Subsystem has multiple partitioning schemes for interfacing with both digital and analog sensors (Figure 4).

The Analog Interface (AIF) is the analog partition scheme, generally used for hybrid solutions where the sensor and the subsystem are manufactured in different technologies. The Parallel Digital Interface (PDIF) is a digital 1-1 partition scheme used for more intelligent (smart front-end) sensors or actuators where the analog-to-digital conversion is done close to the sensor. The Serial Digital Interface (SDIF) is a digital 1-N serial partition scheme for smart front-end sensors or actuators. This interface supports connecting multiple devices to the subsystem using only a limited number of I/O signals.

The Analog to Digital Converter (ADC) interface facilitates connectivity to analog sensors. The integrated I2C and SPI master peripherals provide digital sensor connectivity.

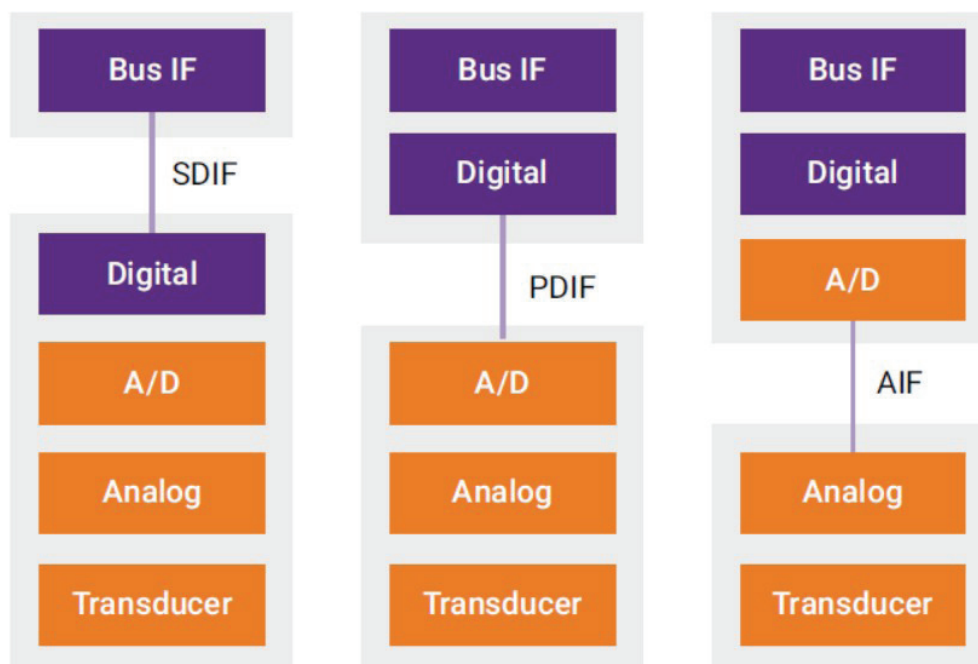


Figure 4: I/O interfaces

SoC Hardware Interface

Hardware integration to an SoC is provided via two ARM® AMBA® AHB™ master bus interfaces for connection to other IP attached to the bus and two AHB slave interfaces for direct access to the closely coupled ARC EM processor memories. If the subsystem is not integrated into an SoC, it can be configured to omit these interfaces. Additional integrated peripherals including UART, PWM, DAC and ARM AMBA APB™ interfaces extend connectivity options for embedded control functions.

Host Interface

The host communication to the ARC Sensor and Control IP Subsystem can be managed via shared memory using one of the AHB interfaces or via a dedicated UART, I²C, or SPI slave peripheral.

Power Management

The ARC Sensor and Control IP Subsystem supports clock switching. All I/O functions and the processor core can be switched off independently. Clock disabling (or enabling) of an I/O function is software controlled. The processor can be put into sleep mode when it runs idle and wakes up on any interrupt.

In a hosted configuration, the lowest power mode of a subsystem node is reached when the host processor stops the node completely and switches off V_{dd} .

Implementation Examples

With the release package customers receive an example sensor control implementation. This is a fully functional design demonstrating a typical use case for the ARC Sensor and Control IP Subsystem:

Use Case—intelligent sensor: This use case demonstrates calibration, filtering and linearization functions required for communicating with analog sensors. It also highlights the use of DSP accelerators and their positive impact on cycle count (translating into performance and energy benefits) and memory footprint.

Demonstrator

An ARC EM Starter Kit (Figure 5) can be separately licensed for demonstration and hardware accelerator evaluation purposes.

The included sensor implementation example can also be mapped on the Starter Kit.



Figure 5: ARC EM Starter Kit

Deliverables

- IPLib installation file which includes:
 - User-configurable hardware (RTL) and software source code (using MIPS' ARChitect IP configuration tool)
 - Complete set of front-end views
 - 2 demonstration applications available as design templates
 - ARC EM IPLib installation file
- Databook (PDF)
- Release notes (PDF)
- ARChitect configuration tool

MIPS ARChitect IP Configuration Tool

- The MIPS ARChitect IP configuration tool is a comprehensive environment for configuring all IP in the subsystem and the generation of RTL and software in line with the chosen configuration. Most configuration options are cross checked for validity during the configuration process. Some options can only be verified during the generation phase. In any case, the designer is protected against creating erroneous designs. During the configuration process the impact of configuration choices on the overall gate count is fed back to the user continuously.

Extension Options

The subsystem is easily extensible via standard AHB and APB bus interfaces. For example, the extensive portfolio of MIPS DesignWare IP can be connected via these interfaces.

Another option is to use the ARC EM processor's APEX interface, which enables designers to add their own user-defined instructions or existing hardware to the processor. This interface is also used internally within the subsystem to connect I/O functions and DSP accelerators.

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