ARC Data Fusion IP Subsystem

Highlights

- Integrated, pre-verified hardware and software IP subsystem
- ARC EM processors with cache and DSP extensions deliver extremely low gate count and highly efficient processing performance
- Extensive library of software DSP functions enable sensor signal processing
- Hardware accelerators boost performance efficiency and reduce power consumption by up to 85%
- Integrated peripherals provide a wide range of SoC connectivity options for SoC/MCUs
- New subsystem options supporting higher performance voice/speech and sensor requirements

Target Applications

- Internet of Things (IoT)
  - Wearable devices
  - Smart energy appliances and hubs
  - Portable medical devices
- Automotive/Industrial
  - Multimedia
  - Industrial automation
- Home Audio
  - Portable speakers
  - Soundbars

Overview

The DesignWare® ARC® Data Fusion IP Subsystem is a complete, pre-verified, hardware and software solution optimized for a wide range of ultra-low power IoT applications. It is designed for fast and easy integration within a larger system context.

The fully configurable ARC Data Fusion IP Subsystem includes the choice of a low gate count and energy-efficient DesignWare ARC EM5D, EM7D, EM9D or EM11D processor for both RISC and DSP processing, accompanied by an extensive collection of I/O functions and fast math (trigonometric) accelerators. The software libraries of the subsystem contain small-footprint drivers for all I/O, plus DSP functions supporting signal processing. The integrated solution is optimized for "always on" data fusion combining sensor, voice, gesture and basic audio processing typically implemented in IoT edge devices.

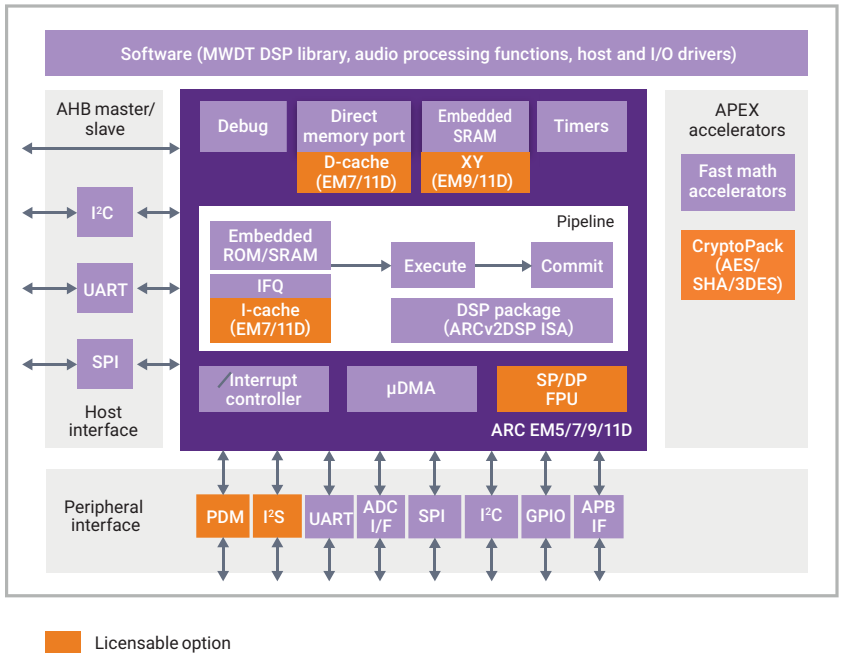

Figure 1: ARC Data Fusion IP Subsystem hardware architecture

The MIPS ARChitect IP configuration tool allows users to fully configure the subsystem. Configuration options include processor settings, number of digital and analog I/O interfaces and use of hardware accelerators. The MIPS MetaWare Development Toolkit can be used for development of user applications that are built upon the ARC Data Fusion IP Subsystem software libraries.

Software Architecture

The ARC Data Fusion IP Subsystem software offering includes a library of DSP functions for signal processing required for data fusion. These functions are supported by native compiler supported instructions within the EMxD processor. Software drivers are also included to ease I/O peripheral integration.

In lieu of an operating system, a lightweight event processing framework is included with the example implementations to quickly get customers started with subsystem integration.

Hardware Architecture

The Data Fusion IP Subsystem provides an optimized hardware architecture consisting of an ARC EM5D, EM7D, EM9D or EM11D processor, tightly coupled digital I/O interfaces via custom registers and a selection of fast math accelerators.

The overall system is highly configurable and extensible (Figure 1).

Key Features

- Efficient RISC/DSP processor
- SoC host & peripheral interfaces
- Hardware accelerators
- Power management
- Software I/O drivers and DSP libraries
- Implementation example
- Demonstrator
- MIPS ARChitect IP configuration tool
- Extension options

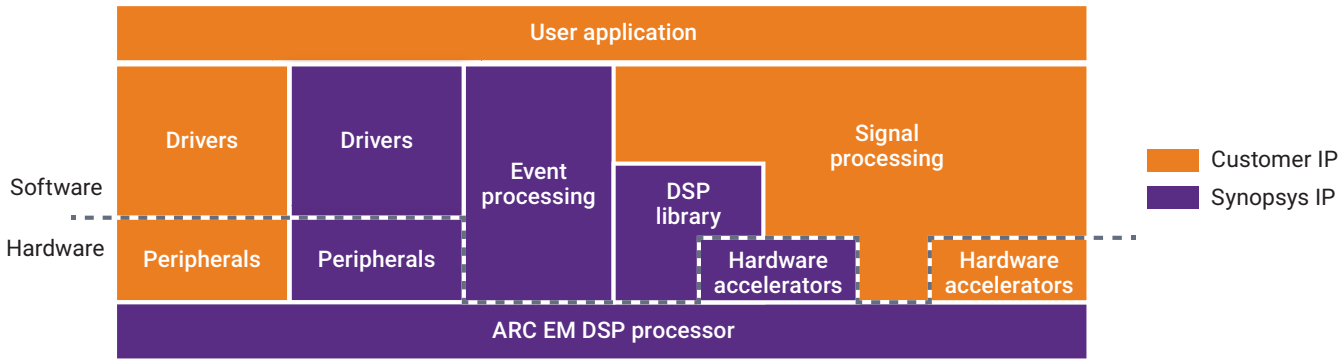

Figure 2: ARC Data Fusion IP Subsystem system view

Efficient Processing

A power-efficient, low gate count ARC EM DSP processor is at the center of the Data Fusion IP Subsystem. All processor core options support up to 2 MB of closely coupled memory (CCM) for both instruction and data, while the

EM7D and EM11D also incorporate up to 32 KB of instruction and data cache for maximum system performance and flexibility. The EM9D and EM11D also provide XY memory for higher DSP bandwidth and performance.

The EM processors are highly configurable and can be optimized for area and performance using a wide range of parameters.

An integrated µDMA controller provides cycle-efficient DMA transfers with low gate count and low power consumption. The µDMA engine supports up to 16 independent channels, and multiple peripheral/memory transfer modes, allowing alternate bus masters to access closely coupled memory (CCM) as well as subsystem peripherals while the EM processor is in one of its low power sleep modes.

Users can add or remove features that improve the efficiency of the core for their application. This includes options such as instruction and data closely-coupled memory configurations, instruction and data caches, IEEE-compliant and single/double precision floating point unit (FPU), address bus width, timers, interrupts, register file structure and debug interface.

Optional Features

- The optional ARC CryptoPack security module can be licensed to accelerate software encryption algorithms such as AES, 3DES, SHA-256 and Elliptical Curve (ECC).
- Floating Point Unit offers single and double-precision math support
- The voice/speech license option provides both hardware and software audio components. Tightly coupled pulse density modulation (PDM) and I2S peripherals enable a wide range of audio devices such as digital microphones and speakers. An audio processing library provides common functions such as gain control, mixer, equalizer, sample rate conversion and more.

SoC Hardware Interface

Hardware integration to an SoC is provided via two ARM® AMBA® AHB™ integrated into a SoC, it can be configured to omit these interfaces.

The Analog to Digital Converter (ADC) interface facilitates connectivity to analog IP such as sensors. Additional integrated peripherals including UART, SPI, I²C and ARM AMBA APBTM interfaces extend connectivity options for embedded control functions.

Host Interface

The host communication to the ARC Data Fusion IP Subsystem can be managed via shared memory using one of the AHB interfaces or via a dedicated UART, I²C, or SPI slave peripheral.

Power Management

The ARC Data Fusion IP Subsystem supports clock switching. All I/O functions and the processor core can be switched off independently. Clock disabling (or enabling) of an I/O function is software controlled. The processor can be put into sleep mode when it runs idle and wakes up on any interrupt.

In a hosted configuration, the lowest power mode of a subsystem node is reached when the host processor stops the node completely and switches off Vdd.

Implementation Example

With the release package customers receive an example ‘always-on’ implementation. This is a fully functional design demonstrating a typical use case for the subsystem:

Use case

Sensor hub (fusion): This use case highlights an example of sensor fusion where multiple digital sensors are connected to the subsystem and their signals are combined to derive an improved calibrated output signal.

Demonstrator

An ARC EM Starter Kit (Figure 3) can be separately licensed for demonstration and hardware accelerator evaluation purposes. The included sensor hub implementation example can also be mapped on the Starter Kit.

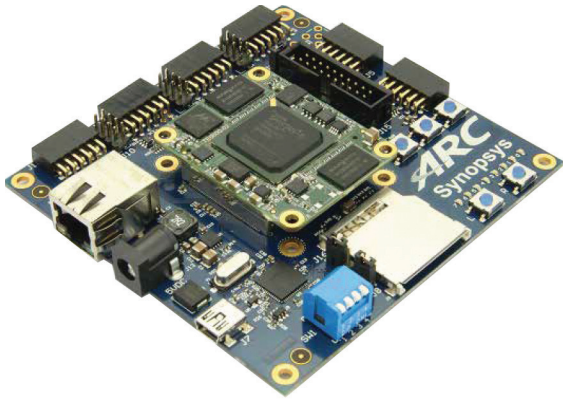

Figure 3: ARC EM starter kit

embARC

MIPS' embARC Open Software Platform is an easily accessible and productive solution for developing ARC processor-based embedded software. It gives software developers online access to a comprehensive suite of free and open-source software that eases the development of code for IoT and other embedded applications. Device drivers, operating systems and middleware ported to and optimized for ARC processors are available for download free of cost from the embARC.org website. The website also provides access to software development tools and documentation as well as user forums to facilitate the sharing of information and expertise among the ARC-based design community.

Deliverables

- IPLib installation file, which includes:
  - User-configurable hardware (RTL) and software source code (using MIPS' ARChitect IP configuration tool)
  - Complete set of front-end views
  - Demonstration application available as design template
  - ARC EM IPLib installation file
- Databook (PDF)
- Release notes (PDF)
- ARChitect configuration tool

MIPS ARChitect IP Configuration Tool

The MIPS ARChitect IP configuration tool is a comprehensive environment for configuring all IP in the subsystem and the generation of RTL and software in line with the chosen configuration. Most configuration options are cross checked for validity during the configuration process. Some options can only be verified during the generation phase. In any case, the designer is protected against creating erroneous designs. During the configuration process the impact of configuration choices on the overall gate count is fed back to the user continuously.

Extension Options

The subsystem is easily extensible via standard AHB and APB bus interfaces. For example, the extensive portfolio of MIPS DesignWare IP can be connected via these interfaces.

Another option is to use the APEX interface of the ARC EM processor, which enables designers to add their own user-defined instructions or existing hardware to the processor. This interface is also used internally within the subsystem to connect I/O functions and DSP accelerators.

About MIPS:

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