DesignWare ARC AXS103 Software Development Platform

Highlights

- Rapid system bring-up for early software development
- Supports ARC HS34, HS36, HS38x2, HS45D, HS47D, and HS48x2 processors
- Broad range of interfaces including USB 2.0 host, HDMI, Ethernet, I²C, SPI, UART, GPIO, and SD card reader
- HapsTrak® 3 extension connector with fast AXI tunnel up to 150 MHz for system prototyping
- Extensible with Digilent Pmod™ Compatible and other peripheral modules
- Software package includes pre-built SMP Linux image, GNU tool chain, MQX RTOS binary, bare metal device drivers and example applications

Target Applications

- SSD controller
- Wireless baseband control
- Switches, routers and home gateways
- Automotive power train control, navigation
- Connected appliances
- Set-top boxes, HD TVs
- Digital cameras

Overview

The DesignWare® ARC® AXS103 Software Development Platform is a complete, standalone platform enabling software development, code porting, software debugging and system analysis. The AXS103 Platform consists of an ARC AXC003 CPU Card mounted on an ARC Software Development Mainboard.
The CPU Card has an associated software package of pre-built operating systems, drivers and example applications.

Readily licensable DesignWare IP has been used to build the ARC Software Development Mainboard, giving the system a rich set of peripherals that can also be implemented in an SoC.

The ARC Software Development Platform can easily be combined with the MIPS HAPS® FPGA-Based Prototyping Solution to enable system prototyping. Additional extension interfaces, such as five Digilent Pmod Compatible connectors, support the integration of other custom and commercially available hardware extensions.

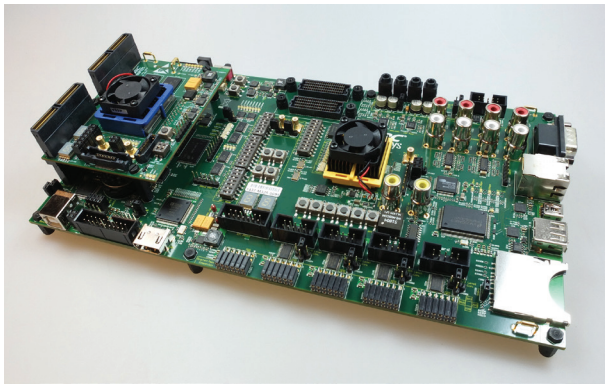

Figure 1: DesignWare ARC AXS103 Software Development system hardware

The ARC Software Development Mainboard contains a rich set of peripheral interfaces including a USB2.0 host, HDMI, Ethernet, audio and several serial protocols. It features an SD card reader and includes multiple memories for storing boot code, application code, operating system and data.

The CPU Card and Mainboard communicate via a high-speed AXI tunnel.

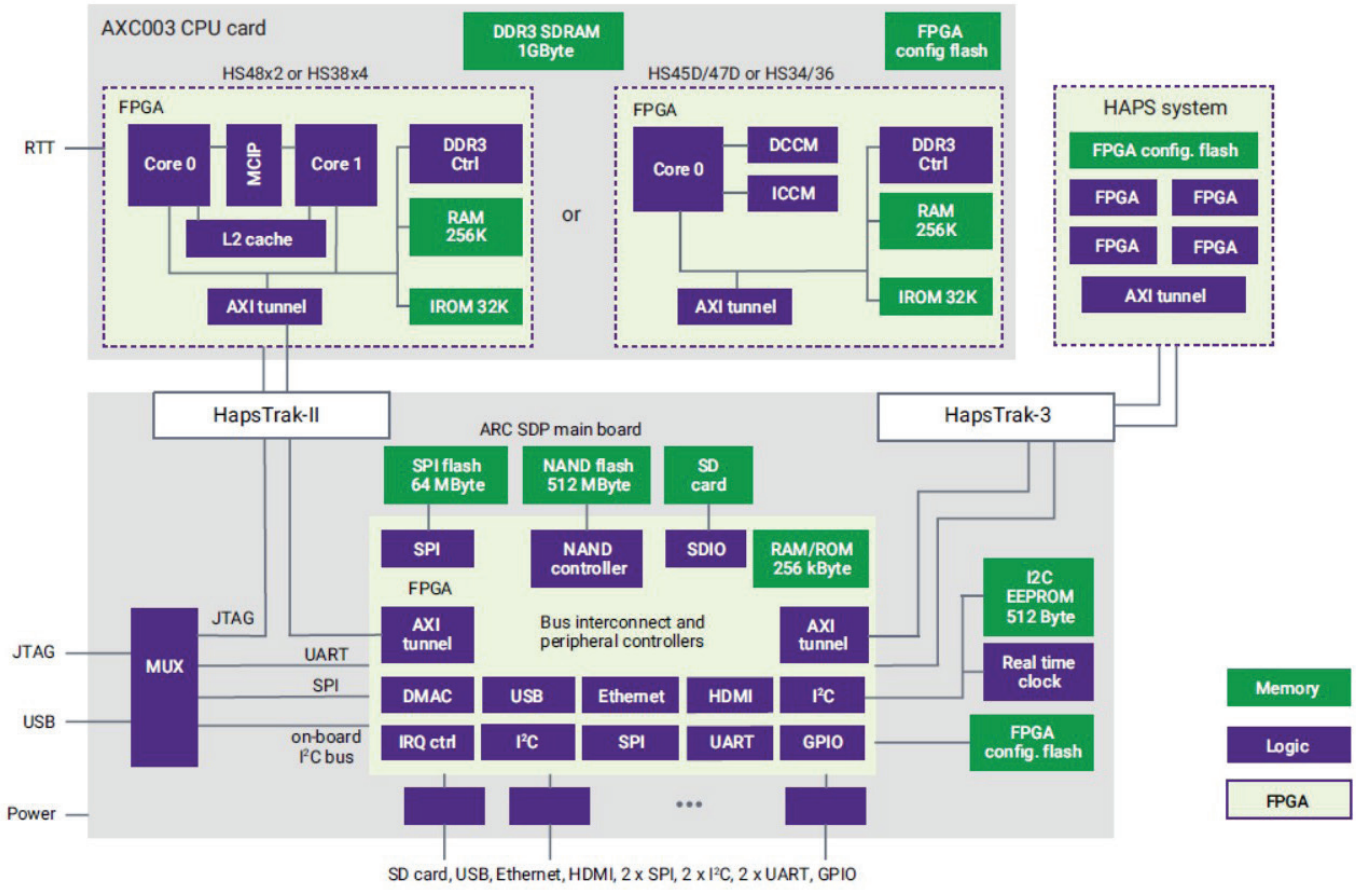

Figure 2. AXS103 hardware block diagram

ARC Software Development Mainboard

The ARC Software Development Mainboard contains the platform peripherals and connections to extend and enhance the ARC Software Development Platform.

Connectivity

The Mainboard supports the following connectivity standards:

- USB 2.0 host interface (type A)
- 10/100 Mbit/s Ethernet
- One I²C master/slave interfaces
- Up to two SPI master interfaces
- Three UARTs
- Up to 40 GPIO pins
- HDMI

USB Data Port

The USB data port provides a convenient interface to your PC. The USB data port can be used for a debug console and as a JTAG interface for debugging. In addition, a command line tool supports reading, erasing or writing the on-board SPI flash and IC EEPROM memories, as well as controlling some on-board devices.

Mainboard Memories

The following memories are available for user applications:

- 64 MByte SPI Flash
- 512 MByte NAND Flash
- 512 Byte I²C EEPROM
- SD card slot

Local memories are available on the ARC AXC003 CPU Card. Additional memories can be added using hardware extensions that can be accessed via the AXI tunnel of the HapsTrak 3 connector or via the SPI or I²C interfaces.

Extension Options

HAPS Extension

A HapsTrak 3 extension connector provides a fast AXI tunnel operating at up to 150 MHz and allows combining the ARC Software Development with MIPS' HAPS FPGA-Based Prototyping Solution. Additional CPU cores, peripherals or other custom hardware can therefore be integrated conveniently and operated at high speed.

RTL source code is provided for implementing the AXI tunnel IP on a HAPS system.

Other Extension Interfaces

Five Digilent Pmod Compatible 2x6 pin connectors support GPIO and serial peripherals (I²C, SPI, UART), thus providing an easy way to integrate commercially available extension modules such as sensors, A/D converters, displays, etc. For increased flexibility the serial peripherals share their pins with GPIO. The pin sharing logic is controlled by the application software.

Additional headers with selectable voltage levels (1.8V, 2.5V, 3.3V, 5.0V) support using other commercial or custom extensions.

Other Mainboard Features

The Mainboard includes a battery-backed real-time clock and two clock oscillators, one 27 MHz oscillator from which the HDMI pixel clock is derived and one 25 MHz oscillator from which all other clocks are derived internally.

Additionally, the following resources are available for user applications:

- Sixteen LEDs
- Six push buttons
- One 9-bit DIP switch

The Mainboard also includes DIP switches and push-buttons to control the boot behavior of the CPU Card.

Debugger Support

The ARC Software Development Mainboard features a USB Dataport combined with a converter, which provides a JTAG debug interface and a debug console via a single USB cable, eliminating the need for dedicated debug probes. However, industry-standard debug probes and cables from Ashling, Lauterbach and Digilent are supported as well. Separate UART interfaces for a debug console are also available.

ARC AXC003 CPU Card

The ARC AXC003 CPU Card includes an FPGA containing a configuration for ARC HS34, HS36 and HS38x2 processors or ARC HS45D, HS47D and HS48x2 processors. Additionally it includes the following resources for user applications:

- 8 LEDs
- 2 seven-segment displays

Table 1 shows an overview of the processor configurations included in the FPGA.

Feature	ARC HS34/HS36	ARC HS38x2	ARC HS45D/HS47D	ARC HS48x2
I-cache (bytes) Associativity Cache-line size	None	64K 2-way 32-bytes	64K (HS47D) 2-way 32-bytes	64K 4-way 64-bytes
D-cache (bytes) Cache-line size	None	64K 32-bytes	64K (HS47D) 32-bytes	64K 64-bytes
Internal memory (bytes)	256K DCCM, 256K ICCM (HS34)	None	256K DCCM, 256K ICCM (HS45D)	
L2 cache (bytes) Associativity Cache-line limit	None	512K 4-way 64-bytes	None	512K 4-way 64-bytes
RTT	Full	Full	Nexus 8bit	None
Core interface	AXI (64 bit)	AXI (64 bit)	AXI (64 bit)	AXI (64 bit)
Core extensions	32x32 multiply Dual and quad MAC Timer0 Timer1 Load/Store Unit Branch Prediction Unit Radix-4 hardware divide Memory Protection Unit Real-time counter	32x32 multiply Dual and quad MAC Timer0 Timer1 Load/Store Unit Branch Prediction Unit Radix-4 hardware divide MMU MCIP	Timer0 Timer1 Load/Store Unit Branch Prediction Unit Memory Protection Unit Real-time counter	32x32 multiply Dual and quad MAC Radix-4 hardware divide Timer0 Timer1 Load/Store Unit Branch Prediction Unit MMU MCIP
Floating-point	Single and double precision Multiply Divide Square root Accumulate	Single and double precision Multiply Divide Square root Accumulate	Single and double precision Multiply Divide Square root Accumulate	Single precision Multiply Divide Square root Accumulate
DSP			Full	None
FastMath			Full	None
Max. CPU freq.	100 MHz	90 MHz	75 MHz	100 MHz

Table 1: CPU configurations on the AXC003 CPU card

The FPGA in the ARC AXC003 CPU card allows processor operation at the following target speeds:

- ARC HS34/HS36: 100 MHz
- HS38x2: 90 MHz

The following memories are available on the CPU Card:

- 2 GByte DDR3 SDRAM
- 256 kByte SRAM

Software

The software delivered as part of the ARC AXS103 Software Development Platform includes a pre-built SMP Linux image (plus the U-bootloader) and the MQX RTOS in binary format. Bare metal and MQX RTOS device driver source code for a subset of the peripherals and example applications. Table 2 shows the operating systems supported by the different ARC HS processors.

	Linux	MQX	Bare metal
HS34/HS36		✓	✓
HS38	✓	✓	✓
HS45D/HS47D		✓	✓
HS48x2	✓	✓	✓

Table 2: ARC HS38 supported operating systems

The MetaWare Development Toolkit, MetaWare Lite tools or ARC GNU Tool Chain provide all the functionality required to create, manage and debug custom applications for the ARC processors.

The ARC GNU Tool Chain (including source code) can be obtained freely from Github (www.github.com, DesignWare ARC).

Boot Scenarios

The ARC Software Development Platform Mainboard includes a preinstalled bootloader that initializes the board, fetches an image from the SPI Flash Memory on the Mainboard, stores it in a local memory (such as DDR3 SDRAM) and then jumps to the target start address to execute the image.Alternatively, a debugger can be used to load an image into a local memory. For this purpose, a DIP switch allows configuring the bootloader to perform the board initialization only and skip image fetching from the SPI flash. The debugger can be connected to the ARC Software Development Platform Mainboard.

The cores can start autonomously after reset, manually via the JTAG debugger, via a push button on the ARC Software Development Mainboard or under software control via a control register.

Deliverables

- ARC AXC003 CPU Card mounted on ARC Software Development Platform Mainboard with pre-installed boot loader
- 100-240V AC power adapter and cable
- USB cable
- Pen-sized plastic DIPSTICK

Downloadable Resources

- Software
  - Pre-built SMP Linux
  - Pre-built U-boot
  - MQX RTOS (in binary format)
  - Peripheral drivers
  - Example applications
  - Command line tool and scripts for board control and memory access
- Documentation
- RTL source code for AXI Tunnel IP

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