# ARC IoT Communications IP Subsystem

## Highlights

- Integrated, pre-verified hardware and software IP subsystem
- ARC EM11D processor with DSP extensions delivers extremely low gate count and highly efficient processing performance
- Hardware accelerators for key communications functions such as Viterbi decoding dramatically reduce cycle counts and energy consumption
- Integrated peripherals provide a wide range of SoC connectivity options for SoC/MCUs
- Digital Front End (DFE) tailored to efficiently connect to multiple partner RF transceivers
- Communications library and optional software stacks provide NB-IoT application layers

## Target Applications

- Internet of Things (IoT)
  - Wearable devices
  - Smart energy appliances and hubs
  - Portable medical devices
  - Object tracking
- Industrial
  - Factory automation
  - Smart city infrastructure

The DesignWare® ARC® IoT Communications Subsystem is an efficient NB-IoT modem solution that incorporates an ultra-low power MIPS DesignWare ARC EM11D Processor, hardware accelerators, integrated peripherals and NB-IoT application software to provide a complete software-defined modem that quickly adapts to continuously evolving standards.

The EM11D's zero-latency XY memory architecture takes advantage of instruction level parallelism and single-cycle 16+16 MAC operations to deliver power-efficient data processing. Integrated ARC Processor eXtension (APEX accelerators) for Viterbi decode and trigonometric functions provide significant reductions in cycle counts, area and power for key low-bandwidth communications kernels

The IoT Communications Subsystem is supported by the MetaWare Development Toolkit, which includes a rich library of DSP functions, allowing software engineers to rapidly implement algorithms from standard DSP building blocks.

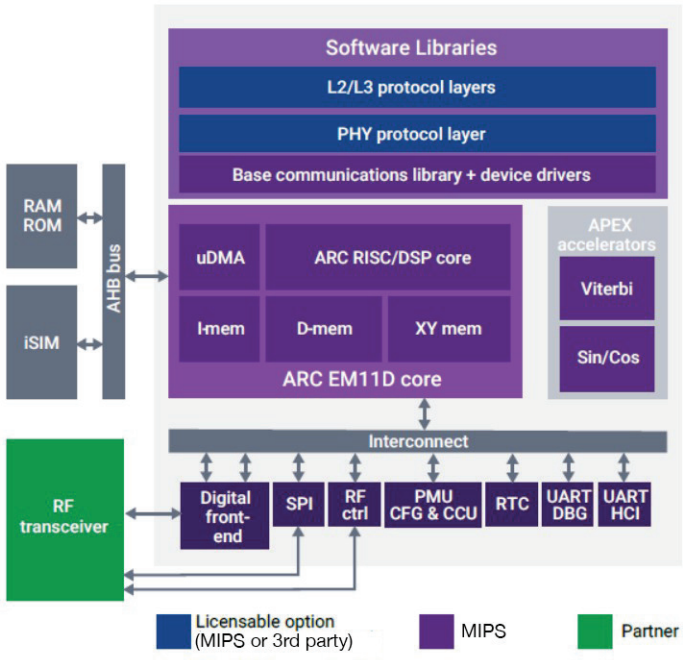


Figure 1: DWC ARC IoT Communications IP Subsystem block diagram

## Key Hardware Features

- ARC EM11D Processor (configurable)
- APEX accelerators for Viterbi and Trigonometry
- Generic digital front-end interface (RF Transceiver via partner)
- AHB infrastructure and peripherals
- Power management

## Key Software Features

- Base communications software library, including code examples
- Low level drivers for DFE, Host IF, USIM, and UART
- Optional: Full Rel13/14 stack including PHY/L2/L3 layers

## Efficient Processing

A power-efficient, low gate count ARC EM DSP processor is at the center of the IoT Communications Subsystem. The processor core supports up to 2 MB of closely coupled memory (CCM) for both instruction and data, and can optionally incorporate up to 32 KB of instruction and data cache for maximum system performance and flexibility. The EM11D also provides XY memory for higher DSP bandwidth and performance. The EM11D processor is highly configurable and can be optimized for area and performance using a wide range of parameters.

An integrated µDMA controller provides cycle-efficient DMA transfers with low gate count and low power consumption. The µDMA engine supports up to 16 independent channels, and multiple peripheral/memory transfer modes, allowing alternate bus masters to access closely coupled memory (CCM) as well as subsystem peripherals while the EM processor is in one of its low power sleep modes.

Users can add or remove features that improve the efficiency of the core for their application. This includes options such as instruction and data closely-coupled memory configurations, instruction and data caches, IEEE-compliant and single/double precision floating point unit (FPU), address bus width, timers, interrupts, register file structure, and debug interface.

## Digital Front End (DFE)

### POWER MANAGEMENT

The ARC IoT Communications IP Subsystem supports clock switching. All I/O functions and the processor core can be switched off independently. Clock disabling (or enabling) of an I/O function is software controlled. The processor can be put into sleep mode when it runs idle and wakes up on any interrupt.

## Additional Licensable Options

To enhance functionality of the ARC IoT Communication Subsystem,  options are also available for license that have been tested and verified with the solution. These options include Floating Point Unit (FPU), an enhanced SecureShield™ security package (ESP), CryptoPack cryptographic accelerator and advanced processor trace.

## Development Tools

To facilitate rapid development with ARC processors and subsystems, they are supported by a complete suite of development tools that generates highly efficient code ideal for deeply embedded applications. The suite of development tools also includes ARC simulators including xCAM and nSIM, and the ARChitect core configuration tool.

For customers enabling the IoT Comms Subsystem's DSP capability, an LLVM- based C++ DSP compiler and comprehensive DSP library are available.

## embARC

MIPS' embARC Open Software Platform is an easily accessible and productive solution for developing ARC processor-based embedded software. It gives software developers online access to a comprehensive suite of free and open-source software that eases the development of code for IoT and other embedded applications. Device drivers, operating systems and middleware ported to and optimized for ARC processors are available for download free of cost from the embARC.org website. The website also provides access to software development tools and documentation as well as user forums to facilitate the sharing of information and expertise among the ARC-based design community.

## Deliverables / Documentation

The following deliverables are provided for the DesignWare ARC IoT Communications IP Subsystem:

- IPLib installation file, which includes:
  - User-configurable hardware (RTL) and software source code (using MIPS' ARChitect IP configuration tool)
  - Complete set of front-end views
  - ARC EM IPLib installation file
- ARC IoT Communications Subsystem Databook (PDF)
- Release Notes (PDF)
- ARChitect configuration tool

## About MIPS:

MIPS by GlobalFoundries delivers software to silicon with RISC-V for building physical AI platforms. MIPS delivers software-hardware co-design, optimized AI, and custom ASSP design and manufacturing. Together with ARC, MIPS delivers the open, standards-based processor IP portfolio for embedded applications. Physical AI is built on MIPS.

For more information, visit **www.mips.com/arc.**