ARC VPXxFS DSP Processors for Automotive

Highlights

- Integrated hardware safety features with minimal area and power impact for full ASIL compliance (ASIL D systematic, up to ASIL C random)
- Four-way VLIW architecture combining scalar and vector operations
- 128-bit, 256-bit, 512-bit, and 1024-bit vector lengths
- 8, 16, and 32-bit integer SIMD engines
- IEEE 754-compliant vector floating point unit option offers single-precision or half-precision operations and advanced math functions
  - Dual vector floating point SIMD pipes
  - Math accelerator
  - FFT accelerator
- Optional data compression support for microscaling OCP MX data types
- Single- and multicore-configured offerings
- Software Test Library (STL) option
- ARC MetaWare tools including a safetycertified auto-vectorizing C/C++ compiler, debugger, simulator, C Runtime, SPEED lightweight multicore runtime library
- Vector DSP and vector linear algebra libraries, Vision SDK and Neural Network SDK

Target Applications

- Automotive driver assistance systems: vision, RADAR and LiDAR processing
- Sensor fusion
- Automotive powertrain and engine management
- Natural language processing
- AI/Machine learning

Overview

The ARC® VPXxFS DSP IP is a family of VLIW/SIMD processors enabling automotive system-on-chip (SoC) designers to accelerate advanced driver assistance systems (ADAS), RADAR and LiDAR sensor processing application development and ISO26262 certification for systems using digital signal processing.

The VPXxFS family supports multiple vector lengths and core configurations:

- 128-bit vector word—VPX2FS (single core), VPX2x2FS (dual core)
- 256-bit vector word—VPX3FS (single core), VPX3x2FS (dual core)
- 512-bit vector word—VPX5FS (single core), VPX5x2FS (dual core), VPX5x4FS (quad core)
- 1024-bit vector word—VPX6FS (single core), VPX6x2FS (dual core), VPX6x4FS (quad core)

The VPXxFS family comes with integrated hardware safety features such as ECC protection for memories and interfaces, safety monitors and lockstep mechanisms, optional Safety Test Library (STL) that achieve the most stringent levels of ISO 26262 functional safety compliance.

To speed application software development, the VPXxFS family is supported by MIPS' safety-certified ARC MetaWare tools, which provide a comprehensive and vector-length agnostic software programming environment that enables code portability among all members of the VPXxFS family. The tool suite includes a safety-certified optimizing C/C++ vector compiler, debugger, instruction set simulator, and a lightweight multicore runtime library (SPEED). Libraries include generic DSP, linear algebra, machine learning kernels, as well as a vision software development kit (Vision SDK).

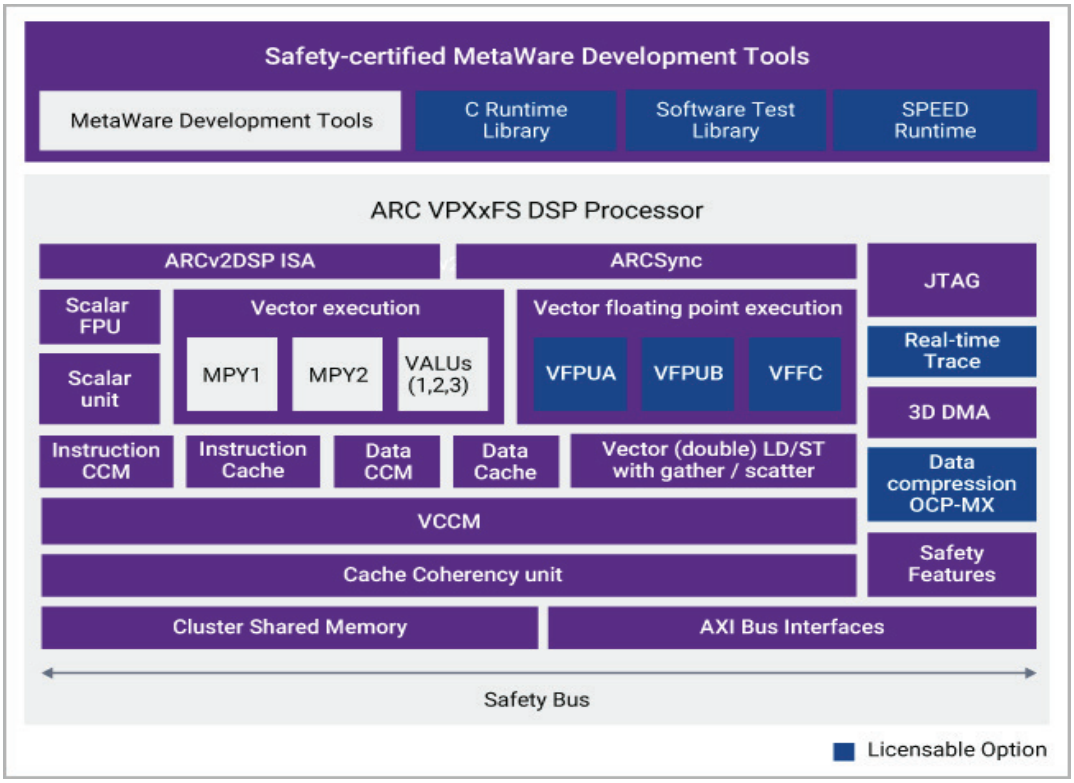

Figure 1: ARC VPXxFS Processor Block Diagram

VPXxFS Safety and Security Features

- ASIL Certified: ISO 26262 ASIL D systematic, up to ASIL C random compliant
- Integrated safety-critical hardware features
- ECC memories
- Diagnostic error injection
- Error classification
- Error checking on core registers and safety-critical registers
- Windowed watchdog timer for each core
- Software diagnostic tests
- Lockstep capabilities for safety-critical modules
- Optional dedicated safety monitor executes safety escalations and diagnostics within the SoC and protects system bring-up
- Licensable option: Safety Test Library (STL), to achieve ASIL B/C compliance
- Safety documentation: FMEDA reports and safety manuals speeds functional safety assessments SAE/ISO 21434 CyberSecurity compliant

ARC VPXxFS Hardware Features

VPXxFS DSP processors feature a 4-way VLIW architecture optimally balanced to achieve high performance with low power consumption. Each VPXxFS DSP core integrates a high-performance 32-bit scalar pipeline and a multi-slot vector processing unit supporting 8-bit, 16-bit, and 32-bit SIMD computations. Each VPXxFS DSP core is capable of executing one scalar and three vector instructions per cycle. The VPXxFS DSPs are supported by configurable instruction and data caches for scalar operations and vector closely-coupled memory (VCCM) with single cycle access for vector processing. Like all ARC processors, the VPXxFS DSPs are highly scalable and configurable, enabling users to tailor them to meet specific performance-power-area (PPA) requirements.

Each ARC VPXxFS DSP core has a scalar register file of up to 32, 32-bit registers. This register file can be constructed from fast, single-cycle access memory or flip-flops, and supports one or two write ports and two read ports. Each VPXxFS core also includes a vector register file with up to 64 registers of varying widths: 1024-bit for VPX6FS, 512-bit for VPX5FS, 256-bit for VPX3FS or 128-bit for VPX2FS.

The VPXxFS DSPs feature scalar 64-bit load double and store double instructions that can be included in the processor at build time. These are single instructions that load or store 64 bits of data to and from register pairs. There is no additional cycle penalty due to the wider and banked data closely-coupled memory (DCCM) that supports non-aligned loads and stores. In addition, the VPXxFS DSPs support vector load double and vector store double instructions that can transmit data up to twice the vector length.

The VPXxFS DSPs' separate instruction and data L1 caches can be independently configured for 4K, 8K, 16K, 32K, or 64KB sizes. The I-cache supports 2- and 4-way associativity, and a 32-, 64-, and 128-byte line size. The caches can be individually configured to support line locking and invalidate, as well as debug visibility. The data cache implements the MOESI protocol and supports cache-to-cache transfers. The ARC VPXxFS DSP processors support 8KB to 128KB of DCCM, and 32KB to 2048KB of vector closely-coupled memory (VCCM) for the vector units. The CCMs are implemented as separate memory spaces and can be accessed every clock cycle.

The VPXxFS DSPs provide an integrated 3-dimensional DMA for flexibly moving data between memories, including external system memory and internal memories like VCCM, DCCM, ICCM and CSM. The DMA supports 1D, 2D and 3D (block) transfers and I/O coherency, and has a configurable number of interfaces to the AXI bus. Together with an integrated coherency unit, optional clustered shared memory, and hardware support for inter-core communication (semaphores, interrupts, message passing), the DMA provides seamless support of integrated VPX multicore configurations. As a licensable option, all VPXxFS family members can process data stored in the OCP-MX microscaling format, with data conversions handled by the DMA on the fly.

The ARC VPXxFS vector lengths are configurable up to 1024-bit (VPX6FS), 512-bit (VPX5FS), 256-bit (VPX3FS) or 128-bit (VPX2FS) with vector support for dual issue of 8x8, 16x16 or 32x32 MAC processing. The DSP SIMD capability can deliver up to 256 8-bit, 128 16-bit, 64 32-bit MACs per cycle. The VPXxFS DSPs support full predication and have scatter/gather instructions and hardware to maximize performance.

Each VPXxFS DSP core can be configured to have up to three parallel floating-point processing pipelines, including two optional IEEE-754 compliant vector floating point units that supports both full- (32-bit) and half- (16-bit) precision floating point operations, with dedicated support for Radix2 and Radix4 for FFT acceleration. The VPXxFS cores also have the option to add a dedicated vector floating point pipe that accelerates an extensive set of math functions including div(x), sqrt(x), 1/sqrt(x), cos(x), sin(x), log2(x), 2^x, e^x.

Cluster Shared Memory

Low-latency shared data memory is optionally available to support information passing and coordination between the multiple DSP cores. This memory is used as a software-managed scratch pad and is configurable from 0 to 8MB. To allow for larger sizes, the memory is internally multi-banked. This memory includes arbitration to support concurrent access from the DSP cores in a multicore configuration.

Real-Time Trace

The optional ARC Real-Time Trace (RTT) unit helps trace executed instructions or program flow and data. ARC RTT generates Nexus 5001 class 3-compliant trace messages. The RTT system can be set up in many different configurations by including the trace generator in the core and the RTT module at build time. ARC RTT can support on- and off-chip memory setups to suit application trace requirements.

Bus Interfaces

The VPXxFS DSP processors have native support for the Arm® AMBA® AXI™ bus protocol. There are multiple AXI bus interfaces and supported bit widths to improve system throughput.

- Standard interface: 64-bit or 128-bit
- Vector direct memory interface (DMI): VPX2FS supports 128-bit, VPX3FS supports 128-bit or 256-bit, VPX5FS and VPX6FS support 128-bit, 256-bit or 512-bit. Up to 4 DMI interfaces are supported in parallel
- DMA interface: VPX2FS supports 4x128-bit, VPX3FS supports 4x128-bit or 4x256-bit, VPX5FS and VPX6FS support 4x128-bit, 4x256-bit or 4x512-bit. Up to 4 DMA channels are supported in parallel

SoC Integration

The VPXxFS DSPs are designed for seamless integration into an SoC. They can be used with any host processor and operate in parallel with the host. The VPXxFS processors include support for synchronization with the host through message passing and interrupts. In addition, part of the VPXxFS memory map can be made visible to other processors.

Comprehensive Software Environment

The ARC MetaWare for Safety Development Tool provides everything needed to program the VPXxFS DSPs. The MetaWare tools include a safety-certified C/C++ compiler, a debugger, and an instruction set simulator (ISS), as well as a wide range of libraries, including DSP and linear algebra, and vision processing. MetaWare tools deliver a high productivity software development environment, including support for a vector-length agnostic programming model allowing for smooth migration of software among all members of the VPXxFS family. Safety-certified versions of both compute and runtime libraries are available as a licensable option.

Compilers and Debuggers	• ASIL-D Ready Certified MetaWare C/C++ Compiler with auto vectorization • MetaWare Debugger	• Develop highly optimized code with an efficient C/C++ compiler for vector and scalar processors • Debug code with a comprehensive source-level debugger and profiler
Simulators	• Fast nSIM Instruction Set Simulator including Near Cycle Accurate Mode (NCAM)	• Use a fast simulator to develop and optimize DSP algorithm software before hardware is available
Libraries and Software Development Kits	• Vector DSP Library • Vector Linear Algebra Library • Machine Learning Library • Vision Library	• Vector-length agnostic libraries provided in source code for optimization to specific core configurations • Linear algebra functions • Machine learning kernels • Computer vision kernels
Runtime Libraries	• C Runtime Library • SPEED	• Accelerate application software development using a module, lightweight runtime library supporting multicore systems • Includes drivers, execution services, interprocessor communications • Enables rapid setup of heterogeneous multicore systems
Neural Network SDK	• Software Development Kit with Neural Network Compiler	• Compiler performs automatic compilation and optimization of neural network models—no manual optimization required • Supports TensorFlow framework; other frameworks (e.g., PyTorch) are supported via ONNX exchange format

Table 1: MIPS ARC MetaWare for Safety Software Development Tools

Documentation

The following documentation is available for the ARC VPXxFS DSPs:

- VPXxFS Release Notes
- VPXxFS Getting Started Guide
- VPXxFS Databook
- ARCv2 Programmers Reference Manual
- Vector DSP and Vector Linear Algebra Library Reference Manuals

Testing, compliance, and quality verification of the ARC VPXxFS DSPs follow a bottom-up verification methodology from block level through system level. Each functional block within the product follows a functional, coverage-driven test plan. The plan includes testing for ARCv2 ISA compliance as well as state- and control-specific coverage points that have been exercised using constrained pseudo-random environments and a random instruction sequence generator.

Deliverables

The MIPS ARC VPXxFS DSPs are delivered as Verilog HDL in the ARChitect IP Library. The HDL is configured and output from the ARChitect IP Configurator tool. A basic testbench of Customer Confidence Tests (CCT) is included.

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