MIPS ARC-V RMX Series Safety Processors

(RMX-110-FS, RMX-510-FS)

Highlights

- Dual-core lockstep safety processors support ISO 26262 automotive safety standards
- Single solution for Automotive Safety Integrity Levels (ASIL) B and D; Supports ASIL D lockstep operation (RMX-110-FS, RMX-510-FS) or ASIL B single-core operation (RMX-510-FS)
- Includes hardware safety features: ECC, integrated user-programmable windowed watchdog timer, end-to-end protection (E2E) for buses/data-path, and lockstep safety monitor
- Support for DSP extensions
- MetaWare Toolkit for Safety with ASIL D Compliant certified compiler
- Extensive safety documentation eases SoC certification process

Target Applications

- ADAS SoCs (safety management)
- Automotive sensors
- Automotive controllers

ARC-V RMX Series Safety Processors for Automotive Applications

The MIPS ARC-V™ RMX Series Safety Processors simplify development of safety-critical applications and accelerate ISO 26262 certification of automotive system-on-chips (SoCs). The ASIL D compliant RMX-110-FS and RMX-510-FS processors are pre-verified, dual-core lockstep implementations including an integrated safety monitor. There is also an option to run the RMX-510-FS core in an independent dual-core "hybrid" mode for ASIL B or non-automotive applications requiring higher performance based on the same design.

The RMX-110-FS and RMX-510-FS processors are supported by comprehensive safety documentation including FMEDA reports and the ARC MetaWare Toolkit for Safety with ASIL D Compliant certified compiler to generate ISO 26262 compliant code.

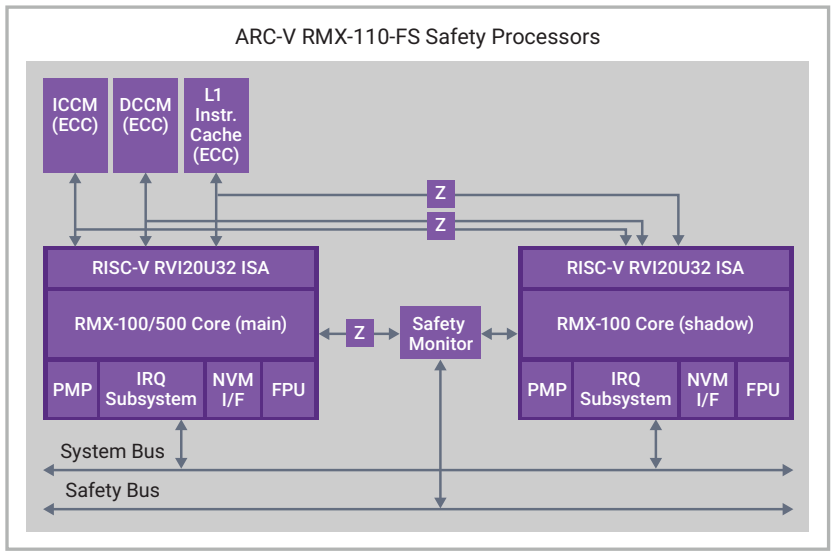

Figure 1: RMX-110-FS Block Diagram

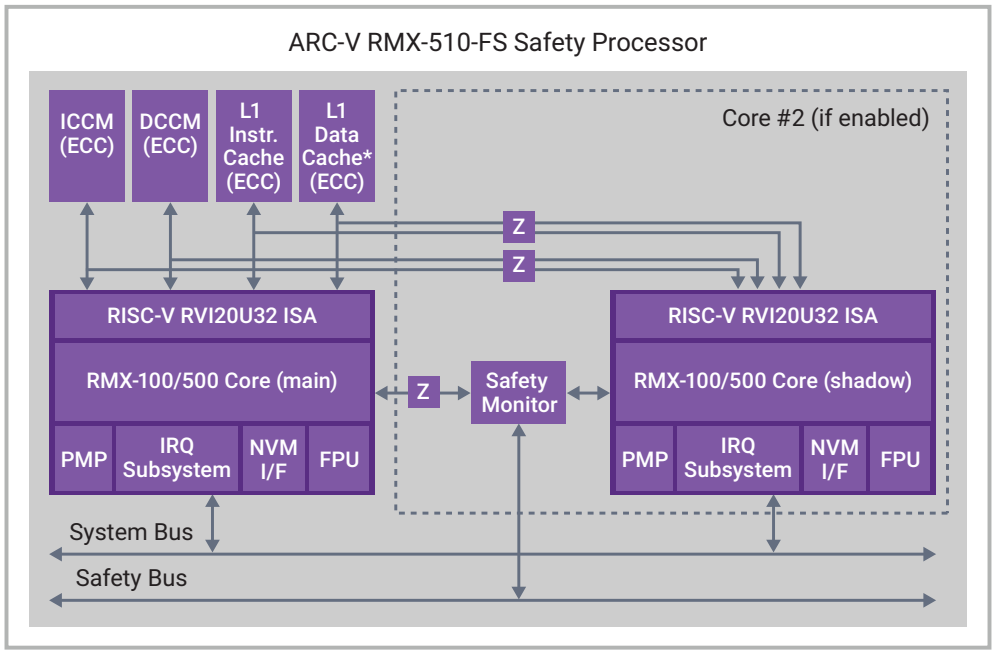

Figure 2: RMX-510-FS Block Diagram

Key Baseline Features

The ARC-V RMX safety processors are 32-bit RISC cores built on the RISC-V ISA and optimized for performance, power, and area efficiency. The processors are aligned to 32-bit ISA profiles defined by the RISC-V standard.

- Single cycle access closely coupled I and D memories (each up to 2MB)
- Up to 64KB of instruction cache and data cache (RMX-510-FS only)
- DSP extensions
- 32x32 unified multiply/MAC unit
- User-configurable program counter
- Configurable zero overhead loop counter
- 32-bit instruction and data busses—Arm® AMBA AXI-5, AHB-5
- Optional single/double precision floating point support
- Optional N-Trace real-time trace support

Hardware Safety Features

The RMX Series safety-enabled processors include hardware safety features that simplify the implementation of safety in an SoC and ease the ISO 26262 certification process. The safety processors support error detection and correction logic (double-bit detect, single-bit correct ECC) for data and address errors on closely coupled memories. Also, hardware stack protection is included to check overflow and underflow of reserved stack space. An integrated watchdog timer helps recover from a deadlock situation.
The integrated memory protection unit (PMP) defines variable regions and assigns access attributes to help protect against malicious or misbehaving code in critical applications.

A tightly coupled architecture is supported such that the interrupt controller, PMP, watchdog timer, and options such as FPU are instantiated within the main and shadow core for full redundancy.

Lockstep Monitor

The RMX-110-FS and RMX-510-FS implement a dual-core lockstep solution that includes an integrated safety monitor. The safety monitor ensures the main core and the shadow core maintain lockstep operation. Support of time diversity is also available, whereas the inputs of one core are delayed by N clock cycles and the outputs of the other core are delayed by the same duration and the results are compared. In this approach, the second core would be performing the same operation N clock cycles after the first one, significantly reducing the probability of a noise pulse hitting both cores and affecting their function.

Additional Licensable Options

To enhance functionality of the ARC-V RMX safety-enabled processors, options are also available for license that have been tested and verified with the solution. These options include a single/double precision Floating Point Unit (FPU) and advanced processor trace module (RISC-V N-Trace).

Development Tools and Software

To facilitate rapid development with ARC-V processors, they are supported by a complete suite of development tools that generates highly efficient code ideal for deeply embedded applications. For developing safety-related software to meet ISO 26262 compliance requirements, certified versions of the MetaWare Development Toolkit and the MetaWare Compiler are available. These products have been certified by SGS-TüV Saar GmbH as ASIL-D Compliant and include a Safety Guide and Safety Manual for using MetaWare tools in safety applications. The suite of development tools also includes ARC-V simulators including nSIM, NCAM and the ARChitect core configuration tool.

For customers enabling the RMX processors' DSP capability, an LLVM- based C++ DSP compiler and comprehensive DSP library are available.

Documentation

The following documentation is available for the MIPS ARC-V RMX-110-FS and RMX-510-FS processors:

- ARC-V ISA Programmers Reference Manual
- ARC-V RMX-110-FS / RMX-510-FS Databook
- ARC-V RMX-110-FS / RMX-510-FS Integration Guide

Additionally, ARC-V RMX safety processors include the following safety work products:

- Dependent Failure Analysis (DFA)
- Design Failure Mode and Effects Analysis (DFMEA)
- Failure Modes Effects and Diagnostic Analysis (FMEDA)
- MIPS IP Quality Manual
- Safety Manual
- Functional Safety Assessment Report (optional)

Testing, Compliance, and Quality

Verification of the ARC-V RMX safety processors follows a bottoms-up verification methodology from block level through system level and includes coverage for systematic and random failures. Use of MIPS tools for fault injection and analysis aid in development of robust and comprehensive diagnostic tests to verify ARC-V processors ability to meet the stringent automotive safety standards.

About MIPS:

MIPS by GlobalFoundries delivers software to silicon with RISC-V for building physical AI platforms. MIPS delivers software-hardware co-design, optimized AI, and custom ASSP design and manufacturing. Together with ARC, MIPS delivers the open, standards-based processor IP portfolio for embedded applications. Physical AI is built on MIPS.

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