ARC-V RMX-500 Series Processors

Highlights

- RISC-V + DSP 32-bit processors for low-power embedded applications
- Based on the RV321 ISA + optional extensions
- 2x 32-bit MAC DSP extensions (RMX-500D) for fixed point and vector operations
- DSP extension instructions overlayed on RISC-V Vector Specification 1.0
- High degree of configurability
- Support for up to 64KB of L1 instruction and data caches
- Support for up to 2 MB of closely coupled memories and direct mapping of peripherals
- Native Arm AMBA® AHB5™ and AXI5 interfaces
- Optional single and multicycle multiplier
- ECC Support
- RISC-V AIA compliant interrupt handling
- N-Trace real-time trace debuggin
- Easy programming support with MIPS MetaWare C/C++ Compiler
- Feature-rich DSP software library for easy algorithm programming (RMX-500D)
- Broad support by third-party commercial and open-source
- Full compatibility with existing RISC-V code base

Target Applications

- Industrial: Motor control, smart metering, smart cities
- Automotive: Sensors, keyless entry, body electronics, safety management
- Consumer: AIoT, wearables
- Storage: consumer SSDs, eMMC, UFS, SD cards
- Networking: LPWAN, M2M, BLE control,

Overview

The MIPS ARC-V™ RMX-500 series processors are optimized for use in embedded applications where power and performance efficiency are key concerns. The DSP enhanced implementation (RMX-500D) adds DSP capability for applications such as IoT wearable devices where the combination of low power and signal processing are required to enable device performance and extend battery life.

The ARC-V RMX-500 processors are based on the RISC-V instruction set architecture (ISA) and supports the RV321 ISA. The processors feature an efficent 5-stage pipeline that provides excellent throughput for embedded applications.

The ARC-V RMX-500 features up to 64KB of level 1 (L1) instruction and data cache and up to 2MB each of closely coupled instruction and data memories (CCM).

The DSP-enhanced RMX-500D cores include an optimized DSP implementation that features support for fixed-point DSP datatypes and vector operations. To enable easy DSP software development, the ARC MetaWare Development Toolkit features a rich DSP software library and the included C/C++ Compiler supports commonly used DSP datatypes for easy algorithm programming.

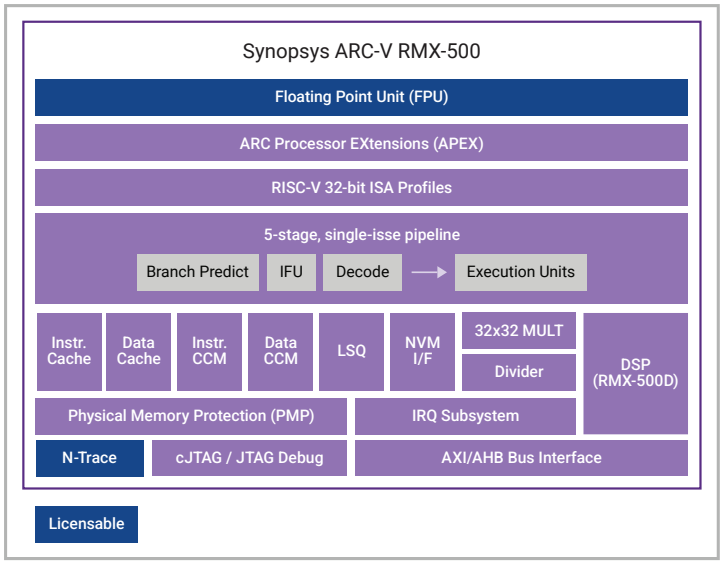

Figure 1: ARC-V RMX-500 Series Embedded Processor Block

Features

- 32-bit RISC-V embedded CPU with a 5-stage pipeline
- DSP-implementation for fixed point and vector to extend the RISC-V baseline (RMX-500D)
- Up to 2MB instruction and data closely coupled memory (CCM)
- 2 KB to 64 KB instruction and data L1 caches
- Architectural clock gating and enhanced sleep instructions
- Supervisor mode for enhanced security
- RISC-V Memory Protection Unit to control access rights to the memory
- Support for World ID's target-side access control / firewalling
- ECC Support
- Integrated watchdog timer
- RISC-V Advanced Interrupt Architecture (AIA) integrated core-level interrupt controller supporting up to 512 interrupts
- Optional APLIC with vector nesting and multi-core support
- Half, single and double precision floating point
- Bfloat16 data type support
- Advanced Platform Level Interrupt Controller (APLIC) supporting up to 1023 wired interrupts
- DSP support (RMX-500D):
  - Unified MUL-MAC unit
  - Fractional data type support
  - Multiple rounding modes
- Native Arm AMBA® AXI5™, AHB5 interfaces JTAG and Compact JTAG (cJTAG) debug interface

Pipeline

The ARC-V RMX-500 cores have a low-latency 5-stage pipeline that is optimally balanced to achieve very low power consumption with excellent embedded performance. It includes a dynamic branch prediction unit based, based on G-share. The pipeline is designed to give longer access to memory, allowing maximum clock speeds at all process nodes. The pipeline is based on the Harvard architecture with separate instruction and data memory storage that can be simultaneously accessed.

RISC-V ISA: Flexible Profile Options

The ARC-V RMX-500 processors leverage the versatile RISC-V instruction set architecture (ISA), offering robust support for RV32I 32-bit ISA. These processors are designed with a high degree of configurability, enabling flexible ISA extension options to efficiently tailor to specific application requirements.

Base ISA / Extension	Description	Default Profile
ISA	RISC-V Base ISA – 32-bit	RV32I
AIA	Advanced Interrupt Architecture	✓
Zifencei	Instruction fence	✓
Zihintpause	Pause hint	✓
Zicbom	Cache block management	✓
Zicsr	CSR instructions	✓
Zce	Compressed instructions	✓
Zba, Zbb, Zbs, Zbc	Bit manipulation instructions	✓
Zicntr	Base counters and timers	✓
Zicond	Integer Conditioning Operations	✓
M	Integer multiply and divide	✓
A	Atomic instructions	Opt
Zfinx, Zdinx	Floating Point (HP, SP, DP)	Opt
World ID	RISC-V World-ID extension	Opt
Supervisor Mode	RISC-V supervisor mode	Opt
RVV	RISC-V Vector Specification 1.0	Opt

Configurable Options

The ARC-V RMX-500 processor cores support a broad range of configurable options, enabling optimization for a specific application's performance, power and size requirements. The included ARChitect configuration tool features a graphical interface and produces verified RTL and synthesis scripts that are compatible with industry-standard design flows. With ARChitect, designers can add or remove features that improve the efficiency of the core for their application, including options such as custom instructions, multipliers, hardware divide, memory configuration, timers, and much more.

Memory Architecture

L1 Cache Memory

The ARC-V RMX-500 processors feature support for instruction and data L1 cache that can be configured for 4 K, 8 K, 16 K, 32 K or 64 K size. The L1 caches are build-time configurable to support 2-way or 4-way set-associativity and a user-selectable line size of 32 or 64 bytes. The caches support line locking offer debug visibility.

Closely Coupled Memories

The ARC-V RMX-500 processor supports up to 2 MB of closely coupled memory (CCM) for both instruction and data. The CCM is implemented as separate memory spaces for the Instruction Closely Coupled Memory (ICCM) and Data Closely Coupled Memory (DCCM) and can be used with cache memory to facilitate maximum system performance and flexibility. Both memory spaces can be accessed every clock cycle and both ICCM and DCCM can be read and written to from outside the core through AHB or AXI target interfaces. Both ICCM and DCCM have support for error-correcting code (ECC) to increase application reliability.

System Architecture and Interfaces

Bus Interfaces

The RMX-500 cores have native support for the Arm AMBA® AXI5, AHB5™ bus protocols. This is a build-time option with the AXI interface as the default selection. These enable the solutions to be easily connected to the SoC infrastructure in most chips without incurring any delay or complication in the bus interface.

DSP Extensions

The MIPS ARC-V RMX-500D processor cores implement MIPS defined ISA extensions that improve DSP performance. The architecture and pipeline are designed to meet the needs of next-generation system-on-chip (SoC) applications and enable the development of extremely power-efficient embedded 32-bit DSP cores.

Error Protection

RMX-500 cores provide support for error protection and caches where present. The different protection schemes may be combined to achieve several levels of protection against malicious or misbehaving code in critical applications. ARC-V RMX-500 supports SECDED single-bit error correction, double-bit error detection (SECDED).

Both odd and even parities are supported. Data-only protection or data and address protection are both supported for ECC.

Interrupt Architecture

The RMX-500 series features the RISC-V Advanced Interrupt Architecture (AIA) with local and system level options. It includes an integrated core-level interrupt controller supporting up to 512 interrupts and optional system-level Advanced Platform Level Interrupt Controller (APLIC).

ARC Processor EXtension (APEX) Interface (RISC-V defined custom extensions)

The processors are designed to be extendable with the addition of custom instructions. These instruction extensions may include more processor and auxiliary registers, new instructions, and additional condition code tests. Custom instructions enable designers to efficiently add their proprietary hardware to the processor to further increase application performance.

Optional Features (Separately Licensed)

- ARC Trace I/F provides real-time trace debugging features for the ARC RMX-500 processor
- DSP extensions (available with RMX-500D processors)
- FPU Floating Point Unit offers half, single and double precision math instructions

Complete Suite of Development Tools

To facilitate rapid development, the processors are supported by a complete suite of development tools via Visual Studio Code IDE Plugin. This includes the MetaWare Development Toolkit that generates performance optimized code ideal for deeply embedded applications.

MIPS offers a suite of GNU tools (ARC GNU) for developers targeting real-time operating systems (RTOS) as well as bare metal systems. The ARC GNU Toolchain includes the GCC compiler and GDB debugger as well as a number of utilities and libraries that make up a complete software toolchain.

Additional development tools are available as part of the RISC-V ecosystem.

Compile	MetaWare Compiler	• Optimize your code for size and performance • Leverage core-specific features to reduce cost and increase performance • Utilize your user-defined instructions to achieve design goals
	GNU GCC Compilerr	• Freely access an open source solution with the GCC compiler
Debug	MetaWare Debugger	• Easily debug multiple targets with the same user interface • Quickly profile hotspots in your code • Use scripting to increase productivity
	JTAG Debuggers	• Efficiently bring-up hardware with tools from ARC 3rd Party Tools and Software partners
	GNU GDB Debugger	• Use the open source GDB debugger to debug real and simulated targets
Deploy	Functional and Cycle-Approximate Simulators	• Develop and debug software before hardware is available • Simulate large programs with very fast ARC-V models • Quickly optimize your software with near cycle-accurate simulation
	Zephyr Real Time OS	• Open source RTOS optimized by MIPS for ARC processors

Documentation

The following documentation is available for the MIPS ARC-V RMX-500 processors:

- ARC-V RMX-500 Series Technical Reference Manual (RMX-500 / RMX-500D)
- ARC-V RMX-500 Series Integration Guide

Testing, Compliance and Quality

Verification of the MIPS ARC-V RMX-500 series processors follows a bottom-up verification methodology from block level through system level. Each functional block within the product follows a functional, coverage-driven test plan.

The plan includes testing for RISC-V ISA compliance as well as state- and control- specific coverage points that have been exercised using constrained pseudo-random environments and a random instruction sequence generator.

Deliverables

The MIPS ARC-V RMX-500 processors are delivered in Verilog HDL in the ARChitect IP Library. The HDL is configurable by the user and output from the ARChitect IP Configurator tool. To test that the product performs as expected, a basic testbench of Customer Confidence Tests (CCT) is included.

About MIPS:

MIPS by GlobalFoundries delivers software to silicon with RISC-V for building physical AI platforms. MIPS delivers software-hardware co-design, optimized AI, and custom ASSP design and manufacturing. Together with ARC, MIPS delivers the open, standards-based processor IP portfolio for embedded applications. Physical AI is built on MIPS.

For more information, visit **www.mips.com/arc.**