MIPS ARC-V RPX-100 Series Processor IP

ARC-V RPX-100, RPX-100V, RPX-105, RPX-105V

Highlights

- Dual-issue, 64-bit RISC-V processors for performance efficient host applications
- Multicore processor versions with up to 16 CPU cores and 12 HW accelerators
- RVA22 and optionally RVA23 RISC-V profile compliant
- Virtualization support through H-extension
- HW configurability
- Support for multi-cycle and non-blocking custom instructions
- Advanced cache architecture:
  - Up to 64 KB L1 instruction and data cache per core
  - Up to 1 MB of unified private L2 cache per core
  - Up to 64 MB of shared L3 cluster cache
- RISC-V Sv39 or Sv48 MMU with HW page table walk and 4 KB to 512 GB page sizes
- RISC-V WorldGuard® security
- Advanced interrupt architecture
- Real-time trace debugging: optional ARC Trace Interface support
- Optional support for RVV and vector crypto extensions, with up to 256-bit wide VLEN and 128-bit wide DLEN

Target Applications

- Industrial: Avionics, medical imaging, factory automation
- Automotive: Zonal controller, powertrain, V2X/V2V/V2I
- Consumer: Baseband control, DVD/set-top Box, VR/AR modems, cameras
- Storage: Storage area networks (SANs)
- Networking: Router, base station

Overview

The MIPS ARC-V™ RPX-100 series processors, which include the RPX-100, RPX-100V, RPX-105, and RPX-105V processor IP, feature a dual-issue, 64-bit superscalar architecture for use in high-performance applications where performance efficiency is required. The cores deliver outstanding performance with minimal power consumption.

The MIPS ARC-V RPX-100 series processors are based on the RISC-V instruction set architecture (ISA). The processors support 40-bit wide physical address space through the RISC-V Sv39/Sv48 MMU.

For applications requiring even higher performance, the multi-core RPX-105 and RPX-105V are available with up to 16 CPU cores and up to 12 hardware (HW) accelerators in the processor cluster, offering scalable solutions for increased computational power and efficiency.

MIPS ARC-V RPX-100V (single core) and RPX-105V (multi-core) processors also include RISC-V extensions (RVV) that are ideal for applications requiring advanced vector processing capabilities.

The MIPS ARC-V RPX-100 series processors feature a highly optimized cache memory system. Each core includes level 1 (L1) instruction and data cache up to 64 KB in size, and up to 1 MB of level 2 (L2) cache. It also supports up to 64 MB of level 3 (L3) cache shared storage capacity that the entire processor can access.

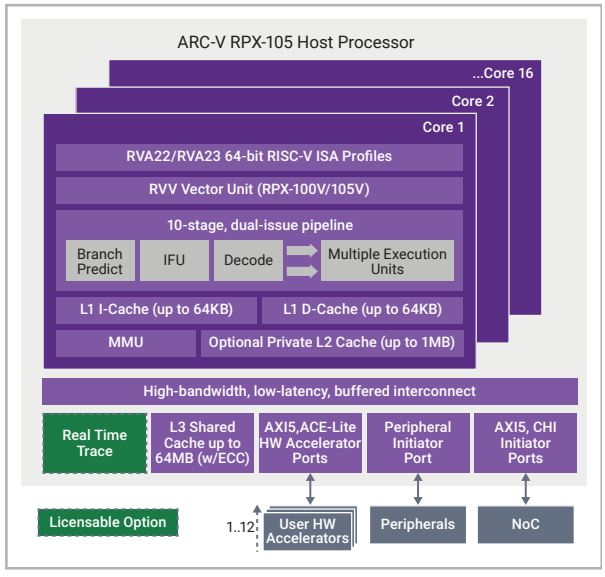

Figure 1: MIPS ARC-V RPX-105 Processor Block Diagram

Features

The MIPS ARC-V RPX-100 series processors are 64-bit RISC-V cores optimized for high performance, low power consumption and area efficiency. The key features are listed below:

- High performance, 64-bit, dual-issue, 10-stage pipeline
- Multicore support for up to 16 CPUs and up to 12 user hardware accelerators per processor cluster
- RVA22 and optionally RV23U64 RISC-V profile compliant
- Enhanced RISC-V Sv39 or Sv48 MMU with support for SMP Linux
- Up to 64KB instruction and data L1 cache per core
- Up to 1MB unified private L2 cache per core
- Up to 64MB cluster shared L3 cache
- Enhanced virtualization with a 3-stage memory protection unit for OS needs (L1), VM isolation (L2) and system-level isolation (L3)
- Up to 2x Advanced Platform Level Interrupt Controllers (APLIC), each supporting up to 1023 wired interrupts for a maximum of 2046 interrupts
- Native ARM® AMBA® AXI5 & CHI interfaces
- ePMP (Physical Memory Protection) with a configurable number of entries
- WorldGuard security
- JTAG and Compact JTAG (cJTAG) debug interface

Dual-Issue Pipeline

The high-performance, 64-bit, dual-issue, 10-stage pipeline is optimally balanced to achieve very high host application performance with efficiency. The pipeline is designed to issue up to two (four with instruction fusion) instructions per clock (in order) and features two-cycle access to memory, allowing the processor to run at higher clock speeds and making it less sensitive to memory size. The pipeline supports out-of-order retirement, sophisticated branch prediction (with early correction of mis-predicted branches) and a patented late-stage ALU (Arithmetic Logic Unit) that improves instruction throughput. Configurable support for 64-bit hardware multiply, vector multiplication, addition and subtraction, and a Radix-4 hardware divider are included. Several separately licensed options are available, including real-time trace debugging.

Multicore Versions

The MIPS ARC-V RPX-100 series processors are available in both single-core and multicore versions. The multicore processor versions support up to 16 CPU cores and up to 12 user-defined hardware accelerators per processor cluster, enabling very high-performance scaling for performance-efficient applications. The advanced multicore interconnect ensures that the CPU cores and hardware accelerators run at maximum throughput and speed. The CPU cores and hardware accelerators can be implemented in their own clock and power domains and can have an asynchronous clock relationship to the other cores and the interconnect, providing greater design flexibility and power efficiency. The CPU cores support full coherency, and the IO coherency is supported with hardware accelerators, ensuring data consistency across the system. Quality of Service (QoS) control is built into the multicore interconnect, allowing users to schedule bandwidth to the CPU cores and hardware accelerators to ensure balanced loading and real-time operation. The shared L3 cache is configurable up to 64MB, supports the CPU cores and user hardware accelerators, and can be kept coherent with other processors and devices within a system-on-chip (SoC).

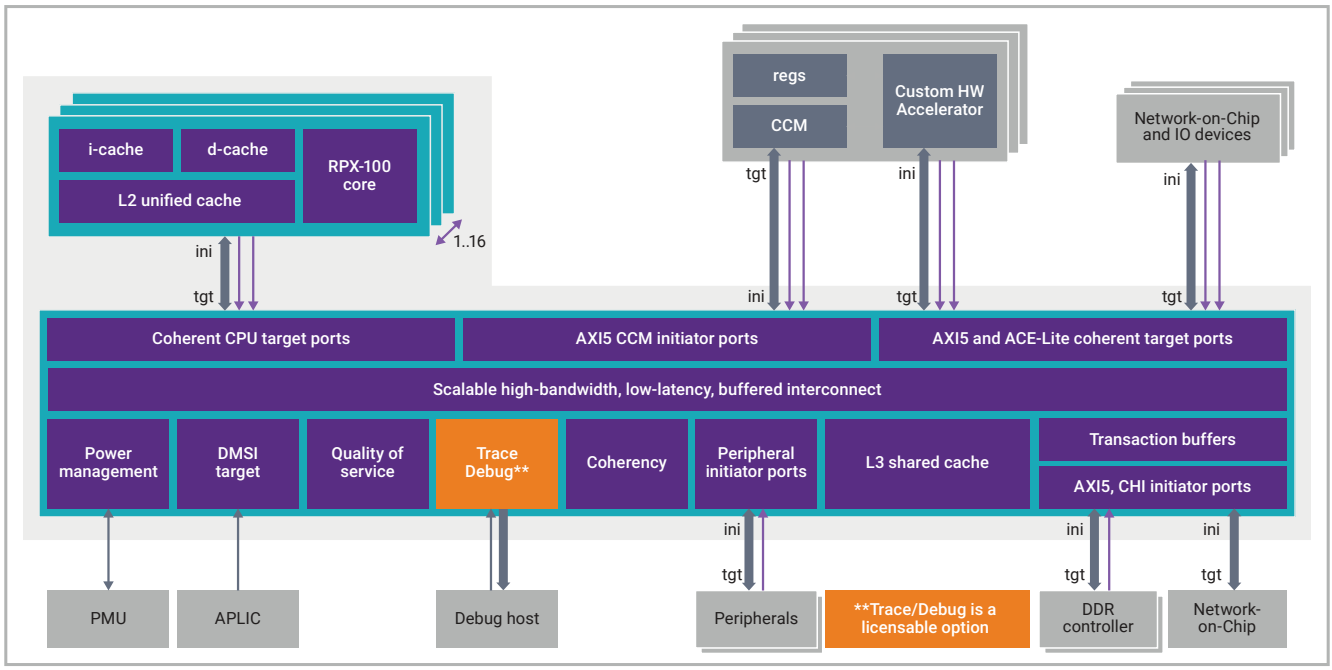

Figure 2: MIPS ARC-V RPX-105 Processor architecture diagram

Configurable Options

The MIPS ARC-V RPX-100 series processors support a broad range of configurable options, enabling designers to optimize performance, power, and size according to the requirements of their applications. The included ARChitect® configuration tool features a graphical interface and generates verified RTL and synthesis scripts that are compatible with industry-standard design flows.

Memory Architecture

L1 Cache Memory

The MIPS ARC-V RPX-100 series processors feature separate L1 instruction and L1 data caches that can be independently configured for 4 KB, 8 KB, 16 KB, 32 KB, and 64 KB sizes, respectively. The L1 instruction cache can be configured as 2-way or 4-way associativity, with a line size of 64 bytes. The L1 caches can be individually configured to support line locking and invalidate as well as to offer debug visibility. The L1 data cache uses MOESI coherency protocol for multicore configurations and supports fast cache-to-cache data transfers.

L2 Cache Memory

Each MIPS ARC-V RPX-100 processor optionally supports up to 1 MB of private coherent, unified L2 cache, providing fast access to instructions and data. The 8-way set associative design minimizes conflict misses, ensuring efficient cache usage. The L2 cache can be used with a single-core or multi-core processor implementation.

L3 Shared Cache Memory

The MIPS ARC-V RPX-100 series processors also support an optional L3 shared cache that can be configured with a capacity of up to 64 MB and an associativity of up to 16. Its multi-banked design ensures that multiple cores can access the cache simultaneously, minimizing contention and maximizing throughput. The hit-under-miss feature and the ability to handle up to 96 outstanding transactions (configurable) allow for efficient and smooth data processing; independent transactions can make individual progress out-of-order.

Memory Management Unit

The MIPS ARC-V RPX-100 series processors memory management unit (MMU) can be configured to support either the Sv39 or the Sv48 virtual memory architecture. A two-level hierarchy of translation lookaside buffer (TLB) caches stores the recent page translations for fast concurrent access. The instruction TLB (ITLB) can be configured to hold 4, 8 or 16 translations for pages of any size. The data TLB (DTLB) can be configured with 8 or 16 translations for pages of any size. The unified L2 TLB is a 4-way set-associative and can be configured to hold up to 2048 translations of 4 KB. In addition to 4 KB pages, Sv39 supports 2 MB and 1 GB sized pages, and Sv48 supports 2 MB, 1 GB, and 512 GB sized pages, each of which must be virtually and physically aligned to a boundary equal to its size.

The L2 TLB is refilled by a hardware page table walker (PTW). To speed up the PTW operation, a translation cache can be configured to hold recently used page table tree structure nodes.

Prefetcher

The prefetcher sits next to the L1 data cache in the ARC-V RPX processor and dynamically identifies stride lengths to prefetch the needed data into the private L2 cache.

System Architecture and Interfaces

Bus Interfaces

The MIPS ARC-V RPX-100 series processors have native support for the AMBA AXI5 and CHI multi-cluster coherent protocol for connection to the network-on-chip (NoC) system. The RPX processor additionally supports up to three AXI5 initiator ports.

Interrupts and Exceptions

The MIPS ARC-V RPX-100 series processors support the advanced interrupt architecture (AIA), enabling advanced and efficient handling of interrupts. Each ARC-V RPX-100 core can receive message-signaled interrupts (MSIs) from an advanced platform-level interrupt controller (APLIC) that ensures real-time delivery of these interrupts. The ARC-V RPX processor can support up to two APLICs, with each APLIC capable of managing up to 1023 wired interrupts, allowing for a total of up to 2046 interrupts. The interrupts are serviced through jump tables and can be triggered by both software and hardware, providing flexibility in interrupt handling.

Additionally, the processor offers a configurable number of always-resident (hardware) interrupt controller contexts. This feature is particularly beneficial for virtual machines, as it facilitates optimized interrupt controller emulation (trap-and-emulate) even in the absence of a dedicated hardware interrupt context.

Hardware Enhanced Virtualization

MIPS provides powerful features for virtualization, including:

- 3-stage memory protection unit for OS needs (L1), for VM isolation (L2) and for system level isolation (L3)
- Fast MPU context switching for accelerated and predictable VM context switching
- Support of virtualized timer and extended virtual IPI (SWI)

ARC Processor EXtension (APEX) Interface for Custom Instructions

The MIPS ARC-V RPX-100 series processors are designed to be extensible with multi-cycle and non-blocking instructions. These instruction extensions may include more processor registers. Custom instructions enable designers to efficiently add their proprietary hardware to the processor to further increase the application performance. The APEX custom instruction interface is available on all RPX cores in a multicore processor separate from and in addition to the user hardware accelerators.

Optional Features (Separately Licensed)

ARC Trace I/F

Provides real-time trace debugging features for the MIPS ARC-V RPX series processors.

Complete Suite of Development Tools

The MIPS ARC-V RPX-100 series processors come with a comprehensive suite of development tools to facilitate rapid development. This suite includes the ARC MetaWare Development Toolkit, which generates performance-optimized code that leverages the highly efficient dual-issue pipeline, making it ideal for high-performance host applications. Additionally, the suite features the ARC nSIM simulators for accurate simulation and the ARChitect configuration tool for easy processor configuration.

MIPS provides a suite of GNU tools (ARC GNU) for developers targeting both Linux operating systems and bare metal systems. The MIPS ARC GNU Toolchain includes the GCC compiler and GDB debugger, along with several utilities and libraries, offering a complete software development environment.

Additional development tools are available as part of the RISC-V ecosystem.

Compile	MetaWare Compiler	• Optimizes code for size and performance • Leverages core-specific features to reduce cost and increase performance • Utilizes user-defined instructions to achieve design goals
	GNU GCC Compiler	• Freely access an open-source solution with the GCC compiler
Debug	MetaWare Debugger	• Easily debugs multiple targets with the same user interface • Quickly profiles hotspots in code • Uses scripting to increase productivity
	JTAG Debuggers	• Efficiently bring up hardware with tools from 3rd party partners such as Ashling, Green Hills and Lauterbach
	GNU GDB Debugger	• Uses the open-source GDB debugger to debug real and simulated targets
Deploy	nSIM Simulator	• Develops and debugs software before hardware is available • Simulates large programs with very fast ARC-V models • Quickly optimizes software with near cycle-accurate simulation
	SMP Linux	• Provides all the benefits of open-source software, including complete source code and a large install base

Table 1: Development tools for MIPS ARC-V processors

Documentation

The following documentation is available for the MIPS ARC-V RPX-100 series processors:

- ARC-V Programmers Reference
- ARC-V RPX-100 Series Technical Reference Manual
- ARC-V RPX-100 Series Integration Guide
- ARC-V APEX Databook

Testing, Compliance and Quality

The verification of the MIPS ARC-V RPX-100 series processors follows a bottom-up methodology from the functional block level through the entire system level. Each block within the product follows a functional, coverage-driven test plan that includes RISC-V ISA compliance and state- and control-specific coverage points. The use of constrained pseudo-random environments and a random instruction sequence generator ensures comprehensive testing, uncovering potential issues and ensuring robust and reliable processor design.

Deliverables

The MIPS ARC-V RPX-100 series processors are delivered in Verilog HDL in the ARChitect IP Library. The HDL is configurable by the user and outputs from the ARChitect IP Configurator tool. A basic testbench of customer confidence tests (CCT) is included to ensure that the product performs as expected.

About MIPS:

MIPS by GlobalFoundries delivers software to silicon with RISC-V for building physical AI platforms. MIPS delivers software-hardware co-design, optimized AI, and custom ASSP design and manufacturing. Together with ARC, MIPS delivers the open, standards-based processor IP portfolio for embedded applications. Physical AI is built on MIPS.

For more information, visit **www.mips.com/arc.**