ARC HS46FS, HS47DFS, and HS48FS Safety Processors

Highlights

- Dual-core lockstep safety processor supports ISO 26262 automotive safety standards
- Certified for ISO 262626 Safety and ISO/SAE 21434 Cybersecurity compliance
- Single solution for Automotive Safety Integrity Level B and D (ASIL B, D Random); Supports both ASIL D lockstep operation or ASIL B single core operation
- Includes hardware safety features: ECC, integrated user-programmable windowed watchdog timer, and safety monitor
- Dual-issue, 32-bit processor for high-performance applications
- Support for DSP instructions (HS47DFS)
- MetaWare Toolkit for Safety with ASIL D Ready certified compiler
- Extensive safety documentation eases SoC certification process

Target Applications

- ADAS
- Radar
- LiDAR
- V2V, V2x networks
- Vision controllers
- Automotive storage

ARC HS4xFS Safety Processors for Automotive Applications

The MIPS ARC® HS46FS, HS46FSx4, HS47DFS, HS47DFSx4, HS48FS, and HS48FSx4 functional safety processors (ARC HS4xFS) simplify the development of high-performance safety-critical applications and accelerate ISO 26262 safety and ISO/SAE 21434 cybersecurity certification of automotive system-on-chips (SoCs). The ASIL D compliant processors feature a pre-verified dual-core lockstep implementation including a safety monitor. Based on the same design, there is also an option to run the cores in performance mode for ASIL B or non-automotive applications achieving higher performance. To achieve ASIL B compliance, the Software Test Library (STL) for HS4xFS is required, which is licensed separately.

Within the processors the interrupt controller, watchdog timer, and options such as cluster DMA and FPU are tightly coupled to the core and are instantiated within the main and shadow core for full redundancy.

The ARC HS4xFS processors are supported with comprehensive safety documentation including FMEDA reports and the ARC MetaWare Toolkit for Safety with ASIL D Ready certified compiler to generate ISO 26262 compliant code.

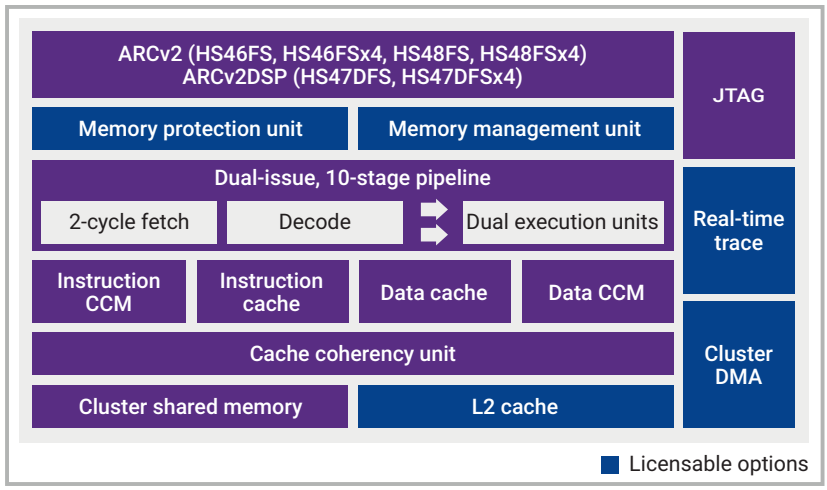

Figure 1: ARC HS4xFS Safety Processor block diagram

Cybersecurity Certification

ARC HS4xFS processors are ISO / SAE 21434 cybersecurity certified, meeting stringent automotive regulatory requirements designed to protect connected vehicles from malicious cyberattacks. The ISO/SAE 21434 standard defines the engineering requirements for cybersecurity risk management, helping to ensure that cyber risks are monitored, detected, and mitigated throughout the vehicle's lifecycle. The certified ARC HS4xFS IP with the Security Risk Analysis (SRA) enables designers to integrate the IP into their system securely to meet ISO/SAE 21434 requirements.

Hardware Safety Features

The ARC HS4xFS processors include hardware safety features that simplify the implementation of safety in an SoC and ease the ISO 26262 certification process. The safety processor supports error detection and correction logic (ECC) for data and address errors on closely coupled memories. Also, hardware stack protection is included to check overflow and underflow of reserved stack space.
An integrated watchdog timer helps recover from a deadlock situation. The integrated memory protection unit (MPU) defines variable regions and assigns access attributes to help protect against malicious or misbehaving code in critical applications.

Lockstep Monitor

The ARC HS4xFS processors implement a dual lockstep solution that includes a safety monitor. The safety monitor provides monitoring to ensure the main core and the shadow core maintain lockstep operation. Support of time diversity is also available, whereas the inputs of one core are delayed by N clock cycles and the outputs of the other core are delayed by the same duration and the results are compared. In this approach, the second core would be performing the same operation N clock cycles after the first one, significantly reducing the probability of a noise pulse hitting both cores and affecting their function.

Features

- High-speed, dual-issue, 10-stage pipeline
- Up to 16 MB instruction and data close coupled memory (CCM)
- 2 KB to 64 KB L1 instruction and data cache
- 64-bit loads and stores
- Register file supports 2 write ports and 2 read ports, and up to 8 contexts
- 32x32 multiplier
- Up to 240 interrupts, with up to 16 configurable preemption levels
- Native Arm® AMBA® AXI™ interface
- JTAG and Compact JTAG (cJTAG) debug interface

Dual-Issue Pipeline

The ARC HS4xFS processors have a high-performance, dual-issue, 10-stage pipeline that is optimally balanced to achieve very high embedded performance with very low power consumption. The pipeline is designed to issue up to two instructions per clock (in order) and features two-cycle access to memory allowing the processor to achieve higher clock speeds and making it less sensitive to memory size. The pipeline supports out-of-order retirement, with a sophisticated branch-prediction logic with very high prediction accuracy and early branch-resolution points to minimize the average misprediction penalty and a late-stage ALU that improves instruction throughput. The processor comes with a 32-bit hardware multiplier (and multiply-accumulate), vector addition and subtraction, and a Radix-4 hardware divider.

L1 Cache Memory

The ARC HS4xFS processors feature separate instruction and data L1 cache that can be independently configured for 2 K, 4 K, 8 K, 16 K, 32 K or 64 K size. The instruction and data cache is fixed to 2-way associativity, and a user-selectable line size of 32, 64 or 128 bytes. The caches can be individually configured to support line locking and invalidate, and to offer debug visibility. For the quad-core configurations (HS46FSx4, HS48FSx4, HS47DFSx4) the L1 data cache implements the MOESI protocol and supports cache to cache transfers.

L2 Cache Memory

The ARC HS4xFS processors offer support for up to 8 MB of L2 cache (separately licensed for HS46FS, HS47DFS). The L2 cache is user configurable up to 8 MB and can be used with both the single-core or multi-core processors. All CPUs in a multicore cluster share the same L2 cache. This cache is designed to run at the same clock frequency as the processor. The coherent L1 caches will work in concert with the L2 cache. The L2 cache is tightly connected to the core(s) through a proprietary low latency bus. The L2 cache interface to the AXI subsystem is configurable to either 64 or 128 bits wide.

Memory Management Unit

The HS4xFS processors can be used with an MMU (separately licensed for HS46FS, HS47DFS), which enables the cores to run sophisticated embedded operating systems that support both SMP and virtual memory. The MMU has a configurable physical address space up to 40 bits, enough for one terabyte of memory. The MMU supports variable page sizes and can concurrently support memory pages in the normal range (up to 16 KB) as well as large pages (up to 16 MB). The primary Translation Lookaside Buffer (TLB) has 1,024 entries and is four-way set associative. The TLB has fully associative micro-TLBs: a four-entry iTLB for instructions and an eight-entry dTLB for data. There is also a 16 entry secondary TLB for super/large pages.

Closely Coupled Memory

The ARC HS4xFSprocessors support 4KB to 16 MB of closely coupled memory (CCM) for both instruction and data. The CCM is implemented as separate memory spaces for the Instruction Closely Coupled Memory (ICCM) and Data Closely Coupled Memory (DCCM). Both ICCM and DCCM have optional support for error-correcting code (ECC).

64-Bit Load and Store

The ARC HS4xFS processors feature double-wide 64-bit load double and store double instructions. These are single instructions that load or store 64-bits of data to and from register pairs. There is no additional cycle penalty due to the wider and banked DCCM that support non-aligned loads and stores.

Interrupts and Exceptions

The HS4xFS processors support up to 240 interrupts and exceptions with 16 nested levels of priority. Designers can select any number of interrupts up to 240 at build time. The interrupts are serviced through a jump table that allows higher flexibility in the location and implementation of the interrupt vectors. Interrupts can be triggered by hardware or software.

Quad-Core Versions

The HS46FSx4, HS47DFSx4, and HS48FSx4 processors are implemented with four cores for applications that require higher performance. The quad-core versions include multiple instantiations of the processor with hardware for intercore message passing, interrupt handling, semaphores and debug. A 64-bit global real-time counter and a global interrupt distribution unit are included to aid in synchronizing multiple threads across the processors. In the multicore versions the cores can be simultaneously and selectively run, halted or reset in any combination by a debugger or a host system. For applications that require ASIL D support, the four cores are lock-stepped with four shadow cores. Quad-core versions can be down-configured to a dual-core version.

Additional Licensable Options

To enhance the functionality of the ARC HS4xFS processors, options are also available that can be separately licensed that have been tested and verified with the solution. These options include MMU, L2 cache, Floating Point Unit (FPU), and advanced processor trace.

Development Tools and Software

To facilitate rapid development with ARC processors, they are supported by a complete suite of development tools that generate highly efficient code for deeply embedded applications. For developing safety-related software to meet ISO 26262 compliance requirements, certified versions of the MetaWare Development Toolkit including the MetaWare Compiler are available. These products have been certified by SGS-TüV Saar GmbH as ASIL D Ready and include a Safety Guide and Safety Manual for using MetaWare tools in safety applications. The suite of development tools also includes ARC simulators including xCAM and nSIM, and the ARChitect core configuration tool.

For customers of the HS47DFS and HS47DFSx4 processors , an LLVM- based C++ DSP compiler and a comprehensive DSP library are available enabling the processors' DSP capabilities.

Documentation

The following documentation is available for the ARC HS4xFS processor:

- ARCv2 ISA Programmers Reference Manual
- ARC HS4x Databook
- ARC HS4x Integration Guide
- ARC HS Safety Manual

Testing, Compliance, and Quality

Verification of the ARC HS4xFS processors follows a bottoms-up verification methodology from block level through system level and includes coverage for systematic and random failures. Use of MIPS tools for fault injection and analysis aid in development of robust and comprehensive diagnostic tests to verify ARC processors' ability to meet the stringent automotive safety standards.

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