MIPS ARC-V RHX Series Safety Processors

(RHX-110-FS, RHX-110V-FS, RHX-115-FS, RHX-115V-FS)

Highlights

- Dual-core lockstep safety processor supports ISO 26262 automotive safety standards
- Single solution for Automotive Safety Integrity Levels (ASIL) B and D; Supports ASIL D lockstep operation or ASIL B single-core operation
- Includes hardware safety features: ECC, integrated user-programmable windowed watchdog timer, end-to-end protection (E2E) for buses/data-path, and lockstep safety monitor
- Support for vector extensions (RVV)
- MetaWare Toolkit for Safety with ASIL D Compliant certified compiler
- Extensive safety documentation eases SoC certification process

Target Applications

- ADAS
- LiDAR
- V2V, V2x networks
- Vision controllers
- Automotive storage

ARC-V RHX Series Safety Processors for Automotive Applications

The MIPS ARC-V™ RHX-110-FS, RHX-115-FS, RHX-110V-FS, and RHX-115V-FS functional safety processors simplify development of high-performance safety-critical applications and accelerate ISO 26262 certification of automotive system-on-chips (SoCs). The ASIL D compliant processors feature a pre-verified dual-core lockstep implementation including an integrated safety monitor. There is also an option to run the cores in an independent "hybrid" mode for ASIL B or non-automotive applications requiring higher performance based on the same design.

The ARC-V RHX Series Functional Safety processors are supported with comprehensive safety documentation including FMEDA reports and the ARC MetaWare Toolkit for Safety with ASIL D Ready certified compiler to generate ISO 26262 compliant code.

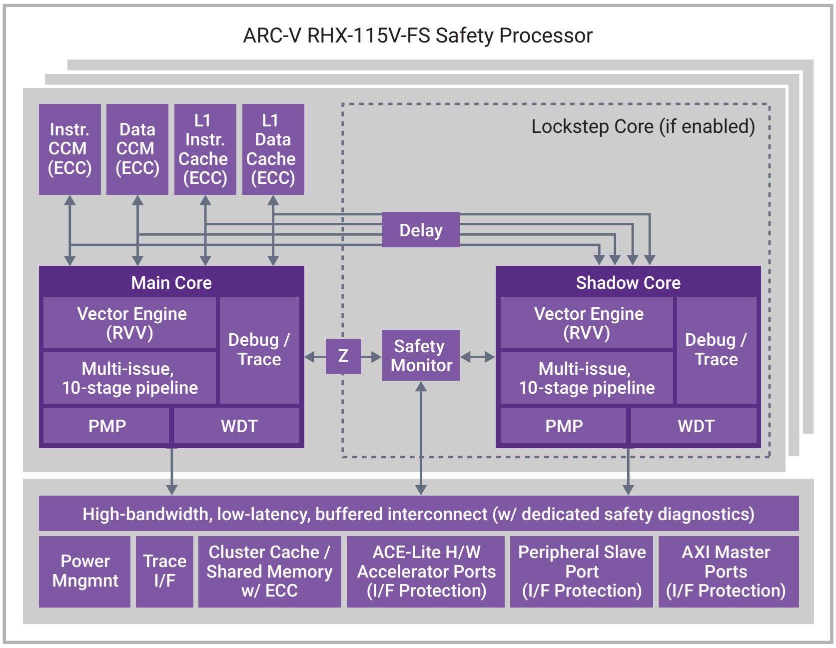

Figure 1: RHX-115V-FS Block diagram

Key Baseline Features

The ARC-V RHX safety processors are 32-bit RISC cores built on the RISC-V ISA and optimized for performance, power, and area efficiency. The processors are aligned to 32-bit ISA profiles defined by the RISC-V standard.

- High-speed, 32-bit, dual-issue, 10-stage pipeline
- Multicore support for up to 16 CPUs and up to 16 user hardware accelerators per processor cluster
- 4 KB to 128 KB instruction and data L1 cache
- Up to 16 MB cluster cache / shared memory
- Up to 16 MB instruction and data closely coupled memory (CCM)
- Real-time enhanced virtualization with 3-stage memory protection unit for OS needs (L1), for VM isolation (L2) and for system level isolation (L3). 128-bit loads and stores per clock
- Radix-4 hardware divider
- Up to 2x Advanced Platform Level Interrupt Controllers (APLIC) each supporting up to 1023 wired interrupts for a maximum of 2046 interrupts
- Native ARM® AMBA® AXI, AHB-Lite interfaces
- JTAG and Compact JTAG (cJTAG) debug interface
- Optional RISC-V Sv32 MMU with support for Linux and SMP Linux
- Optional cluster DMA engine
- Optional N-Trace real-time trace support

Hardware Safety Features

The RHX Series safety-enabled processors include hardware safety features that simplify the implementation of safety in an SoC and ease the ISO 26262 certification process. The safety processors support error detection and correction logic (double-bit detect, single-bit correct ECC) for data and address errors on closely coupled memories. Also, hardware stack protection is included to check overflow and underflow of reserved stack space. An integrated watchdog timer helps recover from a deadlock situation. The integrated memory protection unit (PMP) defines variable regions and assigns access attributes to help protect against malicious or misbehaving code in critical applications.

Within the processors the interrupt controller, watchdog timer, and options such as cluster DMA are tightly coupled to the core and are instantiated within the main and shadow core for full redundancy.

Lockstep Monitor

The RHX safety-enabled cores implement a dual-core lockstep solution that includes an integrated safety monitor. The safety monitor ensures the main core and the shadow core maintain lockstep operation. Support of time diversity is also available, whereas the inputs of one core are delayed by N clock cycles and the outputs of the other core are delayed by the same duration and the results are compared. In this approach, the second core would be performing the same operation N clock cycles after the first one, significantly reducing the probability of a noise pulse hitting both cores and affecting their function. Time diversity buffers include parity checking to reduce single point failures.

Dual-Issue Pipeline

The high-performance, 32-bit, dual-issue, 10-stage pipeline is optimally balanced to achieve very high embedded performance with low power consumption. The pipeline is designed to issue up to two instructions per clock (in order) and features two-cycle access to memory allowing the processor to be run at higher clock speeds and making it less sensitive to memory size. The pipeline supports out-of-order retirement, sophisticated branch prediction (with early correction of mis-predicted branches) and a patented late-stage ALU that improves instruction throughput. Configurable support for a 32-bit hardware multiply, vector addition and subtraction, and a Radix-4 hardware divider are included. Several separately licensed options are available including real-time trace debug, and cluster DMA.

Multicore Versions

The RHX safety cores are available in single-core and multicore processor versions. The multicore processor versions support up to 16 CPU cores enabling very high-performance scaling for high- end embedded applications. The advanced multicore interconnect can support up to 800 GB/s aggregate bandwidth enabling the CPU cores and hardware accelerators to run at maximum throughput and speed. The CPU cores can be implemented in their own clock and power domains and can have an asynchronous clock relationship to the other cores and interconnect. The CPU cores support L1 coherency, and coherency is support between the hardware accelerators, and also between the shared cluster cache and the Network-on-Chip (NoC) if desired. Quality of Service (QoS) control is built into the multicore interconnect that enables the user to schedule bandwidth to the CPU cores and hardware accelerators to insure balanced loading and real-time operation. The shared cluster cache is configurable up to 16MB and supports the CPU cores and and can be kept coherent with memory.

Memory Architecture

L1 Cache Memory

The ARC-V RHX-100 processors feature separate instruction and data L1 caches that can be independently configured for 4K, 8K, 16K, 32K, 64K, or 128K size. The instruction and data cache is fixed to 2-way associativity, and a user-selectable line size of 32, 64 or 128 bytes. The caches can be individually configured to support line locking and invalidate, and to offer debug visibility. For multicore configurations the L1 data cache implements the MOESI protocol and supports coherency and cache to cache transfers.

L2 Cache Memory (optional)

The ARC-V RHX-100 has optional support for up to 16 MB of L2 cluster shared cache. The L2 cache and the shared cluster memory share the 16MB space and the size of each is under the user's control. The L2 cache can be used with a single-core or multicore processor implementations. The coherent L1 caches will work in concert with the L2 cache and all CPU cores and hardware accelerators in a multicore processor can be used with the L2 cache. This cache is designed to run at the same clock frequency as the CPU core. The L2 cache is tightly connected to the core(s) through a proprietary low latency bus. The L2 cluster shared cache feature can be separately licensed for use with the RHX safety cores.

Cluster Shared Memory

The Cluster Shared Memory (CSM) provides a high capacity, high-throughput memory shared by all cores within a multicore processor cluster. It can be used for instructions and data, cacheable and non-cacheable, and sharable and non-sharable address space. The CSM can be accessed by each core using the memory access instructions and instruction fetch operations. The CSM is located in the ARC-V RHX processor cluster and can be mapped to the system memory space. Transactions from components within the cluster, such as processor cores, SCU, hardware accelerators and so on, access the CSM through the IBP interfaces, and transactions from external masters access the CSM through the CSM-DMI interface (if CSM-DMI is configured). The memory macro consists of up to 8 banks so multiple transactions from different interfaces can access the CSM simultaneously. The size of the CSM is build- time configurable, supporting 32 KB, 64 KB, 128 KB, 256 KB, 512 KB, 1 MB, 2 MB, 4 MB, 8MB and 16MB, and memory ECC and parity protection are supported. The CSM shares the memory space with the L2 cluster cache and the maximum size of both combined is 16MB. The CSM clock is gated to reduce dynamic power consumption, and it can be powered down independently while other components and cores are powered-up.

Closely Coupled Memories

The ARC-V RHX safety processors support 512B to 16MB of closely coupled memory (CCM) for both instruction and data. The CCM is implemented as separate memory spaces for the Instruction Closely Coupled Memory (ICCM) and Data Closely Coupled Memory (DCCM), and can be mapped in the global address space. Both ICCM and DCCM have optional support for error-correcting code (ECC) to increase application reliability.

Memory Management Unit (optional)

The ARC-V RHX safety processors feature an optional MMU, which enables the core to run sophisticated embedded operating systems like Linux and SMP Linux. The MMU implements a hardware page table walk and supports variable page sizes with concurrent support for the normal pages (up to 16 KB) as well as large pages (up to 16 MB). The primary Translation Lookaside Buffer (TLB) on the MMU has 1,024 entries and is four- way set associative. The TLB has fully associative micro-TLBs: a four-entry iTLB for instructions and an eight-entry dTLB for data. There is also a 16 entry secondary TLB for super/large pages. The MMU can be separately licensed for use with the RHX series processors.

System Architecture and Interfaces

Register File and Program Counter

The RHX safety-enabled processor cores each support 31 base integer registers with an additional 32 floating registers as a configuration option.

Bus Interfaces

The processors have native support for the AMBA AXI protocol for connection to a NoC. This is a build-time option with the AMBA AXI interface as the default selection. The AXI buses are user configurable with 64- or 128-bit widths to improve system throughput.

Interrupts and Exceptions

The RHX series supports the Advanced Interrupt Architecture (AIA). Individual RHX cores receive Message Signaled Interrupts (MSIs) from an Advanced Platform Level Interrupt Controller (APLIC) with real-time delivery guarantees. The RHX processors support up to two APLICs, each of which handles up to 1023 wired interrupts for a maximum of 2046 interrupts. The interrupts are serviced through jump tables and interrupts can be triggered by software as well as hardware.

Optimized and guaranteed latency of external interrupt delivery - direct or/and MSI mode. Multiple flexible external interrupt controller integration options (tied to the core, cluster level, system level), all provide the same hardware/software interface including native and virtualized environments.

Configurable number of always resident (hardware) interrupt controller contexts for virtual machines. Optimized interrupt controller emulation (trap-and-emulate) for virtual machines without a dedicated HW interrupt context. Redirection of interrupts coming to an idle state VM to hypervisor.

Fast Context Switch Mechanism

Advanced gate-count efficient mechanism for saving / restoring application context, including fast interrupts handling. Provides virtually unlimited number of contexts. Software configurable handling of core registers as well as CSR's.

Real-time Enhanced Virtualization

3-stage memory protection unit for OS needs (L1), for VM isolation (L2) and for system level isolation (L3). Fast MPU context switching for accelerated and predictable VM context switching. Support of virtualized timer and extended virtual IPI (SWI).

ARC Processor EXtension (APEX) Interface (RISC-V-defined custom extensions)

The processors are designed to be extendable with the addition of custom instructions. These instruction extensions may include more processor and auxiliary registers, new instructions, and additional condition code tests. Custom instructions enable designers to efficiently add their proprietary hardware to the processor to further increase application performance. The APEX custom instruction interface is available on all RHX CPU cores in a Multicore processor and is separate from and in addition to the user hardware accelerators.

Low-Latency Auxiliary Port

The low-latency auxiliary port offers fast access to on-chip peripherals and memory. The port supports single-cycle read and write register access bringing these peripherals close to the processor and significantly reducing the latency that accompanies accessing peripherals and memory over a multi-layer AMBA bus interface. In addition, system performance is improved because this processor- to- peripheral bus traffic is moved to the auxiliary bus. The auxiliary port can support all peripheral registers on an SoC.

Optional Features (Separately Licensed)

- ARC Trace I/F provides real-time trace debugging features for the ARC-V RHX processor
- Cluster DMA programmable memory access controller
- Memory Management Unit (RISC-V Sv32 MMU)

Development Tools and Software

To facilitate rapid development with ARC-V processors, they are supported by a complete suite of development tools that generate highly efficient code for deeply embedded applications. For developing safety-related software to meet ISO 26262 compliance requirements, certified versions of the MetaWare Development Toolkit and the MetaWare Compiler are available. These products have been certified by SGS-TüV Saar GmbH as ASIL D Ready and include a Safety Guide and Safety Manual for using MetaWare tools in safety applications. The suite of development tools also includes ARC-V simulators including NCAM and nSIM, and the ARChitect core configuration tool.

Documentation

The following standard documentation is available for the ARC-V RHX safety processors:

- ARC-V Programmers Reference Manual
- ARC-V RHX Safety Processors Technical Reference Manual
- ARC-V RHX Series Integration Guide
- ARC-V APEX Databook

Additionally, ARC-V RHX safety processors include the following safety work products:

- Dependent Failure Analysis (DFA)
- Design Failure Mode and Effects Analysis (DFMEA)
- Failure Modes Effects and Diagnostic Analysis (FMEDA)
- MIPS IP Quality Manual
- Safety Manual
- Safety Case Report
- Functional Safety Audit Report
- Functional Safety Assessment Report
- Software Tool Qualification Report

Testing, Compliance, and Quality

Verification of the ARC-V RHX safety processors follows a bottoms-up verification methodology from block level through system level and includes coverage for systematic and random failures. Use of MIPS tools for fault injection and analysis aid in development of robust and comprehensive diagnostic tests to verify ARC-V processors ability to meet the stringent automotive safety standards.

About MIPS:

MIPS by GlobalFoundries delivers software to silicon with RISC-V for building physical AI platforms. MIPS delivers software-hardware co-design, optimized AI, and custom ASSP design and manufacturing. Together with ARC, MIPS delivers the open, standards-based processor IP portfolio for embedded applications. Physical AI is built on MIPS.

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