

DesignWare ARC AXC003 CPU Card

Highlights

- ARC CPU Card used on ARC AXS103 Software Development Platform
- FPGA implementation provides early access to advanced processor cores
- Supports ARC HS34, HS36, HS38x2, HS45D, HS47D, and HS48x2 processors
- 2 Gbyte of DDR3-SDRAM and 256 kByte on-chip SRAM
- Software package includes a pre-built SMP Linux image, GNU Tool Chain, MQX RTOS binary, bare metal device drivers and example applications

Target Applications

- SSD controller
- Wireless baseband control
- Switches, routers and home gateways
- Automotive power train control, navigation
- Connected appliances
- Set-top boxes, HD TVs
- Digital cameras

Overview

The DesignWare® ARC® AXC003 CPU Card is the daughter card used on the ARC AXS103 Software Development Platform. It plugs directly into AXS103 Software Development Platform Mainboard to create a complete software development platform for ARC code development. The AXC003 CPU Card includes an FPGA that supports four ARC CPU configurations with the following operational speed targets:

ARC HS34/HS36	100 MHz
ARC HS38x2	90 MHz
ARC HS45D/HS47D	100 MHz
ARC HS48x2	75 MHz

The FPGA on the ARC AXC003 also includes 256 kByte of on-chip SRAM and the AXC003 CPU Card features 1 GByte of DDR3-SDRAM.

The deliverables include a software package containing pre-built operating systems, drivers and application examples. Code development is made easy using the MetaWare Development Toolkit, MetaWare Lite tools or the ARC GNU Tool Chain.

Together, the ARC AXC003 CPU Card and the ARC AXS103 Mainboard form a powerful development platform enabling real-time software development and validation, code porting, software debugging and system analysis.

The ARC AXC003 CPU Card, as part of the ARC AXS103 Software Development Platform, enables the use of advanced ARC CPU cores as a daughter card for the MIPS HAPS® FPGA-Based Prototyping Solution.

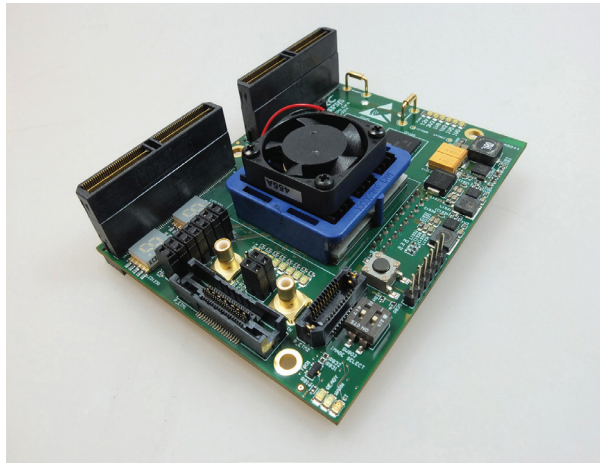


Figure 1: DesignWare ARC AX003 CPU Card

Feature	ARC HS34/HS36	ARC HS38x2	ARC HS45D/HS47D	ARC HS48x2
I-cache (bytes) Associativity Cache-line size	None	64K 2-way 32-bytes	64K (HS47D) 2-way 32-bytes	64K 4-way 64-bytes
D-cache (bytes) Cache-line size	None	64K 32-bytes	64K (HS47D) 32-bytes	64K 64-bytes
Internal memory (bytes)	256K DCCM, 256K ICCM (HS34)	None	256K DCCM, 256K ICCM (HS45D)	
L2 cache (bytes) Associativity Cache-line limit	None	512K 4-way 64-bytes	None	512K 4-way 64-bytes
RTT	Full	Full	Nexus 8bit	None
Core interface	AXI (64 bit)	AXI (64 bit)	AXI (64 bit)	AXI (64 bit)
Core extensions	32x32 multiply Dual and quad MAC Timer0 Timer1 Load/Store Unit Branch Prediction Unit Radix-4 hardware divide Memory Protection Unit Real-time counter	32x32 multiply Dual and quad MAC Timer0 Timer1 Load/Store Unit Branch Prediction Unit Radix-4 hardware divide MMU MCIP	Timer0 Timer1 Load/Store Unit Branch Prediction Unit Memory Protection Unit Real-time counter	32x32 multiply Dual and quad MAC Radix-4 hardware divide Timer0 Timer1 Load/Store Unit Branch Prediction Unit MMU MCIP
Floating-point	Single and double precision Multiply Divide Square root Accumulate	Single and double precision Multiply Divide Square root Accumulate	Single and double precision Multiply Divide Square root Accumulate	Single precision Multiply Divide Square root Accumulate
DSP			Full	None
FastMath			Full	None
Max. CPU freq.	100 MHz	90 MHz	75 MHz	100 MHz

Table 1: CPU configurations on the AX003 CPU card

ARC Processor Configurations

Table 1 shows an overview of the ARC processor configurations included with the AXC003 CPU Card. All processors support:

- Actionpoints for hardware breakpoints and watchpoints
- Smart tracing for instruction execution and history inspection

Memories

In addition to the closely coupled memories of the CPU cores (such as ICCM and DCCM, shown in Table 1), the CPU Card includes the following system memory components:

- 1 Gbyte DDR3-SDRAM
- 256 kByte on-chip SRAM

Non-volatile memories, an SD card slot and other memory extension options are available on the ARC AXS103 Software Development Platform Mainboard.

Software

The software delivered as part of the ARC AXC003 CPU Card includes pre-built SMP Linux image (plus the U-boot bootloader) and the MQX RTOS in binary format. Bare metal and MQX RTOS device driver source code for a subset of the peripherals and example applications. Table 2 shows the operating systems supported by the different ARC HS processors.

	Linux	MQX	Bare metal
HS34/HS36		✓	✓
HS38	✓	✓	✓
HS45D/HS47D		✓	✓
HS48x2	✓	✓	✓

Table 2: ARC HS38 supported operating systems

The MetaWare Development Toolkit, MetaWare Lite tools or ARC GNU Tool Chain provide all the functionality required to create, manage and debug custom applications for the ARC processors.

The ARC GNU Tool Chain can be obtained freely from GitHub (www.github.com, DesignWare ARC).

Boot Scenarios

The ARC AXS103 Software Development Platform includes a pre-installed bootloader that initializes the board, fetches an image from the SPI Flash Memory on the Mainboard, stores it in a local memory (such as DDR3 SDRAM), and then jumps to the target start address to execute the image.

Alternatively, a debugger can be used to load an image into a local memory. For this purpose a DIP switch allows configuring the bootloader to perform the board initialization only and skip image fetching from the SPI flash. The debugger can be connected to the ARC Software Development Platform Mainboard.

The cores can start autonomously after reset or manually via the JTAG debugger, using a push button on the ARC Software Development Platform Mainboard or under software control through a control register.

Deliverables

- AXC003 CPU Card

Downloadable Resources

- Software
 - Pre-built SMP Linux image
 - Pre-built U-boot
 - MQX RTOS (in binary format)
 - Peripheral drivers
 - Application examples
- Documentation

About MIPS:

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