MIPS ARC Software Test Library

Highlights

- ARC STL implements a hardware safety mechanism for ARC FS Processors using software driven testing approach
- STL is usually a required safety mechanism for non-lock-stepped variants of ARC FS Processor IP
- Enables random permanent hardware fault coverage up to ASIL-C together with hardware-based safety mechanisms as per ISO26262:5
- Co-developed with hardware safety mechanisms to achieve optimal hardware PPA characteristics in combination with minimal runtime software overheads
- Runs transparently to user applications, enabling boot time and mission mode testing
- ISO26262:6 certified for usage in up to ASIL-D applications

The MIPS ARC® Software Test Library (STL) for ARC Processors is a hardware safety mechanism, as defined in the ISO 26262 standard, implemented in software; it is designed to detect random permanent (stuck-at) hardware faults during the execution of mission software. A Software Test Library, also known in the automotive industry as Software Built-In Self-Test (SBST) is an external safety mechanism that, in combination with other processor safety mechanisms, provides the required level of Single Point Failure Metric (SPFM) diagnostic coverage with respect to the target ISO 26262 ASIL. The table below shows possible target ASIL for various MIPS ARC functional safety (FS) processor families.

ARC Processor Family	Target ASIL
ARC EM FS	ASIL B
ARC HS FS	ASIL B
ARC EV7x FS	ASIL B / ASIL C
ARC VPX FS	ASIL B / ASIL C

Table 1: Target ASIL for various ARC FS Processor families

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The MIPS ARC STL is a static software library with C language API that consists of a collection of diagnostic routines. Each diagnostic routine is intended to cover a specific processor block or specific processor function. The other outcome of running STL is triggering and propagating faults to other hardware safety mechanisms such as ECC, watchdog timers, MPU, and MMU when those are used as safety mechanisms.

ARC STL is designed for boot time as well as mission mode testing scenarios. All STL tests are implemented as non-intrusive tests for minimal interference with application software and don't require external execution context save/restore procedures. Mission mode software calls the full set of STL tests within one diagnostic time interval, which is a system defined parameter.

The entire test set can be split into compile-time configurable chunks to achieve the required balance between runtime overheads and introduced extra latency for the entire system. The exact set of STL tests as well as STL runtime performance characteristics depends on the hardware configuration of the ARC FS Processor and the target safety case.

MIPS ARC STL is certified as a hardware safety mechanism against requirements defined in ISO 26262:5 together for the select hardware configurations of ARC FS Processor IP. ARC STL is also certified as a software library as per ISO 26262:6 for use in safety relevant applications of up to ASIL-D. The exact list of certified hardware platforms is specified in the ARC STL release notes. Other variants of MIPS ARC FS Processor IP are subject to ARC functional safety tailoring process and STL tailoring is a part of this process.

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