SYNOPSYS®
Silicon to Software™

ARC µDMA Controller for DesignWare ARC EM Processors

Highlights

- Tightly coupled to the ARC EM core for low latency
- Energy-efficient DMA transfers, 70% less energy than equivalent load/store operation
- 1 to 16 independent programmable DMA channels (configurable)
- User-programmable prioritization scheme for all channels
- Concurrent operation with the CPU
- Software and hardware triggered DMA transfers
- Two addressing modes
- Up to 5 data transfer modes (configurable down to 1)
- Internal and external interrupt support
- Supports Link-List multi-block transfers

Target Applications

- Mobile
- IoT
- Storage

Area- and Power-Efficient DMA Controller for ARC EM Processors

A DMA controller improves efficiency by moving data around in a system without the involvement of the CPU. The µDMA controller is a fast, low energy optimized option for DesignWare® ARC® EM Processors to allow fast DMA transfers with low gate count and low power consumption. The µDMA engine is tightly coupled to the ARC EM core interfaces to achieve low latency and cycle-efficient DMA transfers optimized to reduce energy.

The Designware ARC EM µDMA controller is configurable to support from one to 16 independent DMA channels. It includes a user programmable prioritization scheme for all channels. The DMA transfers can be triggered by software or hardware and can proceed concurrently with CPU operation or when the CPU is in a sleep state. The µDMA has two addressing modes and from one to five transfer modes with internal and external interrupt support.

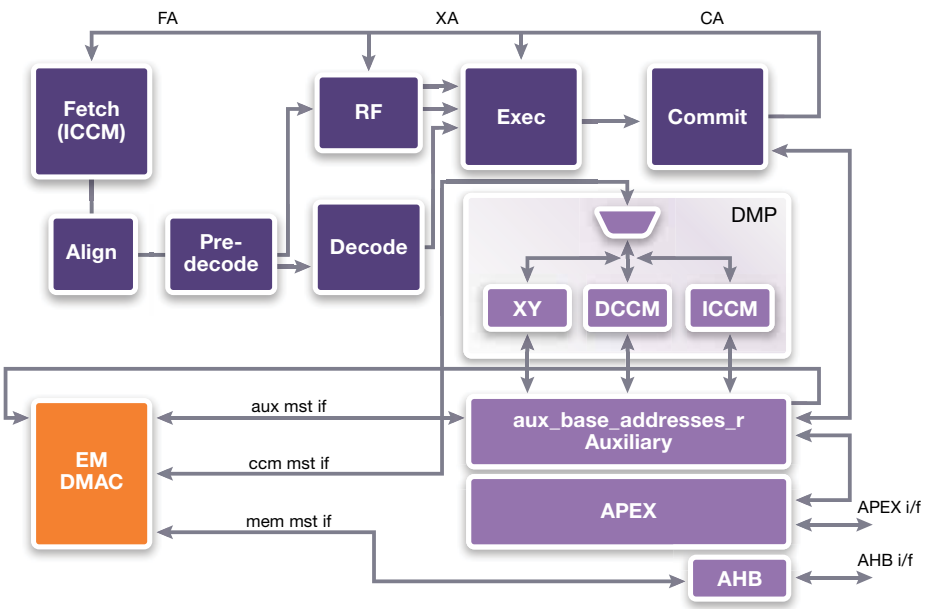
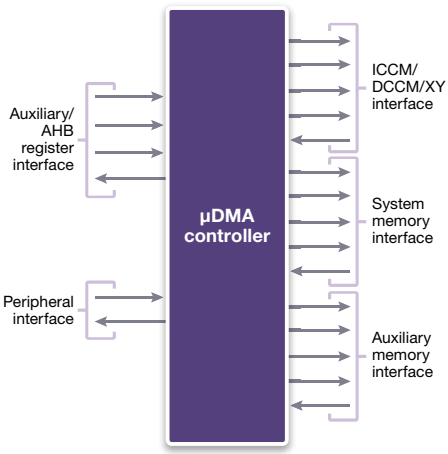


Figure 1: ARC µDMA block diagram

ARC EM µDMA Operation

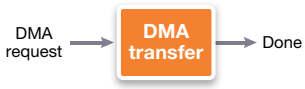
The closely coupled memory (CCM) interface supports DMA data transfer to and from ICCM0, ICCM1, DCCM or XY memory, and a DMA peripheral interface is provided to allow external devices (such as a DesignWare I²C peripheral) to initiate DMA transfers through the ARC Auxiliary Interface. Each channel is assigned a separate request/acknowledge signal interface.



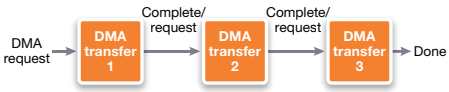
µDMA data transfer characteristics

- µDMA transfer size allows up to 8k bytes of data to be transferred per DMA request
- µDMA transfer data widths supported include 32-bits, 16-bits, or 8-bits (DMA source/destination starting addresses must be aligned according to transfer data width)
- µDMA transfers modes
  - Memory → Memory (where memory can be CCM, XY, system or peripheral memory)
  - ARC Auxiliary Interface → Memory
  - Memory → ARC Auxiliary Interface
  - ARC Auxiliary Interface → ARC Auxiliary Interface
- Option to raise an interrupt on the completion of a block transfer
- µDMA addressing modes include address increment by byte, half word, word or no increment

Single block transfers are used to copy a block of data. When a DMA request is asserted, a data block is transferred based on the information defined in the DMA channel's control and address registers. When the transfer completes, the DMA control register must be re-written and the DMA request must be asserted again to the same channel to trigger another DMA transfer.



Link-List DMA transfers are used to connect a series of separate single block transfers into one operation. When the first block transfer completes, the address pointer DMALLP[n] is used to locate the next DMA channel register set (descriptor) in memory to use. The registers are read in and the new data transfer is started. The fetching of descriptors and the subsequent execution of block transfers continue until a terminating descriptor is read.



The ARC EM µDMA is specifically optimized to reduce energy consumption in systems with ARC EM processors.

Documentation

The following documentation is available for the DesignWare ARC µDMA Option for EM:

- ARCv2 ISA Programmers Reference Manual
- ARC EM Databook
- DesignWare ARC EM Integration Guide

Testing, Compliance and Quality

Verification of the ARC EM µDMA follows a bottom-up verification methodology from block-level through system-level. The module follows a functional coverage-driven test plan, which includes testing for ARCv2 ISA compliance as well as state- and control-specific coverage points that have been exercised using constrained pseudo-random environments and a random instruction sequence generator.

ARC EM Processors

The ARC EM processors, built on the ARCv2 instruction set architecture (ISA) are designed to meet the needs of next-generation system-on-chip (SoC) applications and enable the development of a full range of 32-bit processor cores – from low-end, extremely power-efficient embedded cores to very high-performance host solutions that are binary compatible and designed with common pipeline elements. ARC EM processors can be precisely targeted to meet the specific performance and power requirements for each instance on a SoC, while offering the same software programmer's model to simplify program development and task partitioning.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired interface IP, wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP Prototyping Kits, IP Virtual Development Kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market.

For more information on DesignWare IP, visit http://www.synopsys.com/designware. Follow us on Twitter at http://twitter.com/designware_ip.

SYNOPSYS®
Silicon to Software™

Synopsys, Inc. • 690 East Middlefield Road • Mountain View, CA 94043 • www.synopsys.com

10/15.RP.CS6568.