ARC MetaWare MX Development Toolkit

Highlights

- Comprehensive set of tools and software enabling the use of vector DSP and AI in automotive, machine learning (ML) and vision applications
- Easy to use Neural Network (NN) SDK, optimized for embedded inference applications, automatically reduces computation, memory, and bandwidth requirements
- Complete product solution: C/C++ compiler with linker and assembler, debugger with GUI and profiler
- Complete simulation tool flow with Instruction Set Simulator and Near Cycle Accurate profiling. Platform level simulation for early software development
- Industry-leading code density performance; optimizing and vectorizing compilers for efficient software development
- Extensive DSP programming support with scalar and vector C/C++ programming models and a collection of pre-optimized compute libraries including DSP, linear algebra, and standard math libraries
- Computer vision library to accelerate vision algorithms and applications
- Also enables software development on Synopsy ARC-V™ and ARC EM/HS processor IP families

Overview

The Synopsys ARC® MetaWare MX Development Toolkit is a complete suite of tools, SDKs, runtime software and libraries that provide everything needed to program the ARC NPX Neural Processing Unit (NPU) IP and ARC VPX DSP IP. The product provides a modular solution to accelerate embedded, DSP, ML and vision applications.

The following table shows the main components of the Synopsys ARC MetaWare MX Development Toolkit:

Component	Description
NN Compiler	ONNX-based compiler supports quantization and optimizations of advanced NN models, partitioning models and tiling between VPX and NPX, optimized code generation for multi-core and multi-cluster VPX and NPX processors
NN Simulation Models	Functional and performance NN simulations models for architectural exploration and early software development
Documentation and reference examples	• Databooks, datasheets, programing user guides,reference manuals and application notes • User space library to access NPX offload capabilities • Example integration into standard open-source NN runtimes • NPX communication Linux reference driver
VPX/NPX Firmware	Complete firmware optimized for inference run of compiled NN models. Provides software interface to a host processor
MetaWare Development Toolkit	Integrated toolkit provides optimizing compilers for ARC processors, debugger, compute libraries and instruction-based simulator with performance information. Optimized vector DSP, linear algebra (BLAS/LAPACK) and vision libraries

Table 1: Synopsys ARC MetaWare MX Development Toolkit components

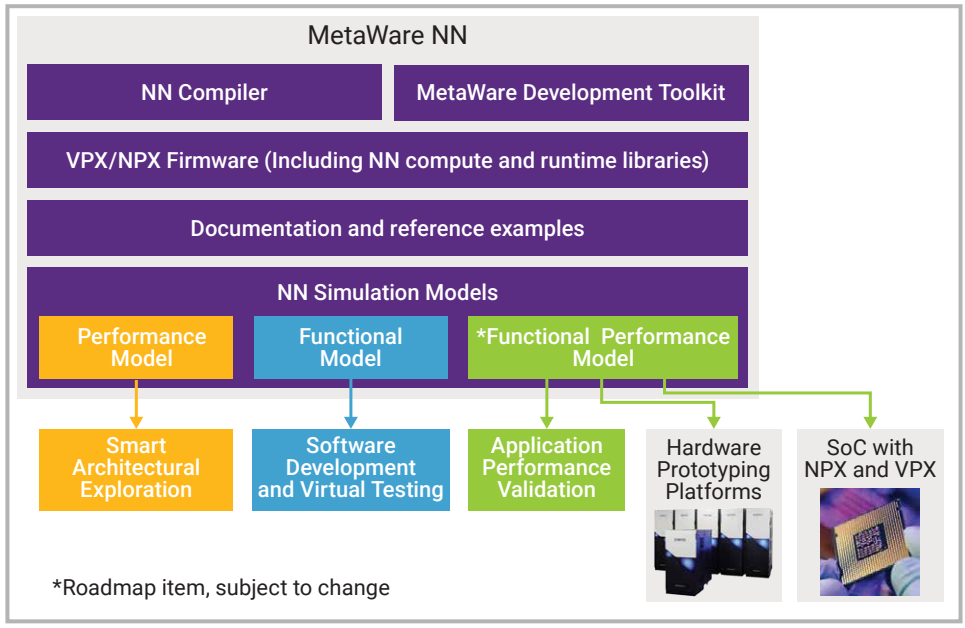

Figure 1: Synopsys ARC MetaWare MX Development Toolkit Overview

ARC MetaWare NN Compiler

The Synopsys ARC MetaWare NN Compiler (Figure 2) is designed to compile, validate and deploy high performance machine learning (ML) applications on ARC processors. It provides integration capabilities with ML frameworks such as ONNX, TensorFlow, Pytorch, TFLite, and Keras. The NN Compiler takes a trained NN model in ONNX format and translates it to an optimized execution format that can be loaded and interpreted by the MetaWare NN Runtime.

- Optimizes code by automatically reducing computation, memory and bandwidth requirements
- Offers a unified API to allow easy deployment of applications using the optimized network
- Includes benchmarking and profiling capabilities, providing users with full featured AI workflows
- The generated code can be simulated with Functional Model for accuracy checking as well as Performance Model with cycle information
- Optional integration into Virtual Platform frameworks (e.g. Platform Architect, Virtualizer)
- Generated code can run on multiple development platforms such as Zebu H/W Emulator and HAPS FPGA board

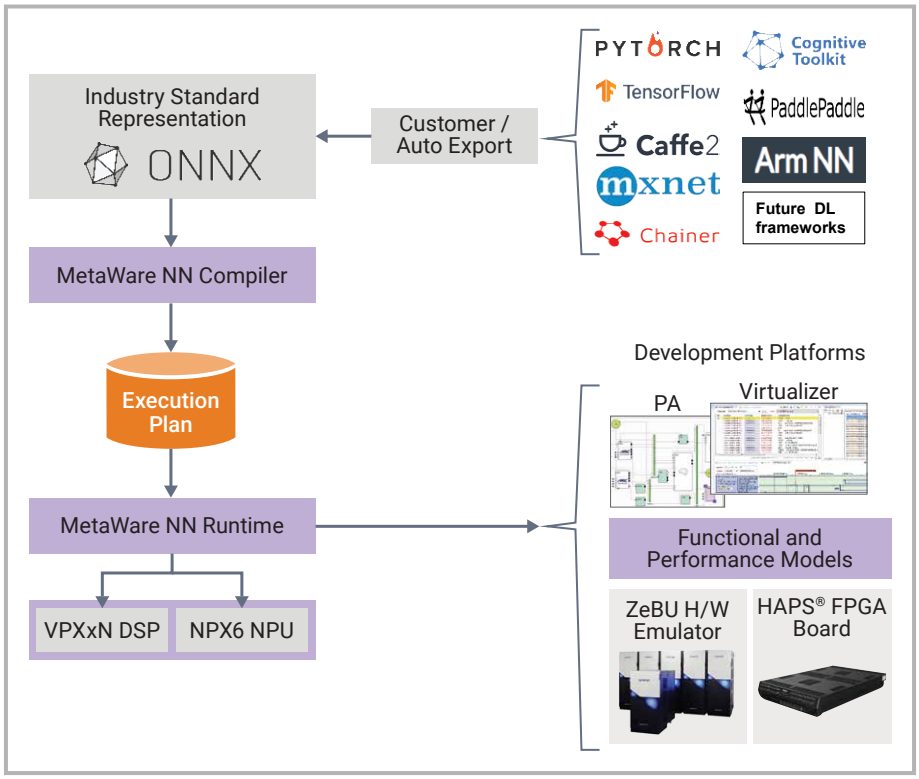

Figure 2: Synopsys ARC MetaWare NN Compiler top-level Diagram

NN Simulation Models

Performance Model (APM/PM)

- Static performance estimation report
- Produced during NN compile
- No functional or compute output
- Used for early performance benchmarking of NN models and architecture exploration by silicon vendors
- Optionally integrate into Synopsys Platform Architect via SystemC interface to create a virtual platform

Functional Model (FM)

- Executable model which produces bit-exact outputs
- Runs natively on x86 workstation
- Used for accuracy checking
- Optionally integrate into Synopsys Virtualizer via SystemC interface to create a virtual platform

*Functional Performance Model (FPM)

- Executable model which produces bit-exact outputs and timing estimates
- Runs natively on x86 workstation
- Used for system integration benchmarking
- Optionally integrate into Synopsys Platform Architect via SystemC interface to create a virtual platform

*Roadmap item, subject to change

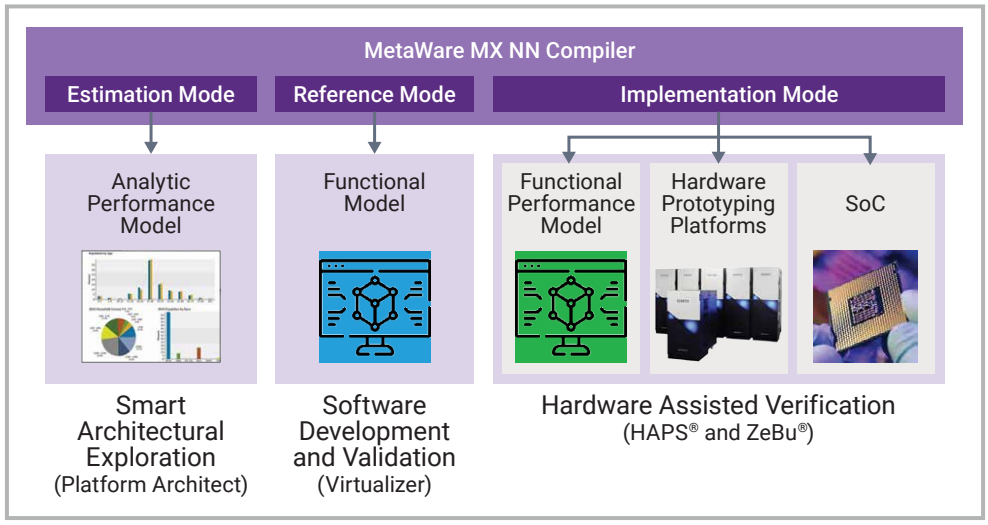

Figure 3: MetaWare MX NN Compiler Simulation Models

Note: Simulation models for VPX are included in Synopsys ARC MetaWare Development Toolkit. Please refer to the nSIM Instruction Set Simulator with Near Cycle Accurate Mode (NCAM) which enables early application software development and optimization before hardware is available.

ARC MetaWare Development Toolkit

The Synopsys ARC MetaWare Development Toolkit is included as part of the MetaWare MX Development Toolkit. It contains all the components needed to support the development, debugging and tuning of embedded applications for Synopsys ARC and ARC-V processors.

For more details, please refer to the Synopsys ARC MetaWare Development Toolkit datasheet.

Simulink Model-Based Design Support

The Synopsys ARC MetaWare Development Toolkit is compliant with Simulink® Model-Based Design flow. Model-based design takes advantage of Synopsys ARC processor Hardware Support Packages. It allows users to develop algorithms at a higher level of abstraction. The Simulink Model-Based Design flow automatically generates Vector DSP Library C code with highly optimized library function calls to the ARC processor. The Vector DSP Library and Vector Linear Algebra Library are used as code replacement libraries to produce the optimized code that can then be compiled and run on the ARC processor.

About Synopsys IP

Synopsys is a leading provider of high-quality, silicon-proven semiconductor IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, interface IP, security IP, embedded processors, and subsystems. To accelerate IP integration and silicon bring-up, Synopsys' IP Accelerated initiative provides architecture design expertise, hardening, and signal/power integrity analysis. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market.

For more information on Synopsys IP, visit synopsys.com/ip.

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