ARC MetaWare Development Toolkit

Highlights

- Complete solution: C/C++ compiler with linker and assembler, debugger with GUI and profiler, ARC nSIM instruction set simulator with NCAM and with IDE single
- Unified tool chain for all Synopsys Processor IP easing the transition between users of ARC CPUs and ARC-V CPUs
- Industry-leading code density performance
- Complete C++ language support including standard template library, compute libraries, SPEED runtime and OpenCL C language support
- Extensive DSP programming support with DSP Library, fixed-point API and native fixed-point data types
- Multicore debugging support
- Support for customer defined instructions and extensions enabled by ARC processor EXtensions (APEX) technology
- Automatic Overlay Management for memory constrained systems (for specific ARC processors only)
- Supports Ashling Microsystems' Opella-XD and Ultra-XD probes and trace pods
- Supports Digilent JTAG cables for JTAG and cJTAG
- Certified version ready for use in developing safety-related software to ISO 26262, up to ASIL-D, TCL 1 is available

Overview

The Synopsys ARC® MetaWare Development Toolkit builds upon a 25-year legacy of industry-leading compiler and debugger products. It is a complete solution (Figure 1) that contains all the components needed to support the development, debugging and tuning of embedded applications for Synopsys ARC and ARC-V™ Processor IP. The tool chain supports the complete family of ARC-V processors, including the 32-bit ARC-V RMX embedded processors, the 32-bit ARC-V RHX real-time processors, the 64-bit ARC-V RPX host processors. The MetaWare Development Toolkit also supports ARC Processors, from the high-speed ARC HS family, the deeply embedded ARC EM family, and the ARC VPX DSP family, to the general-purpose ARC 600 family and the ARC 700 family for high-performance applications (Table 1).

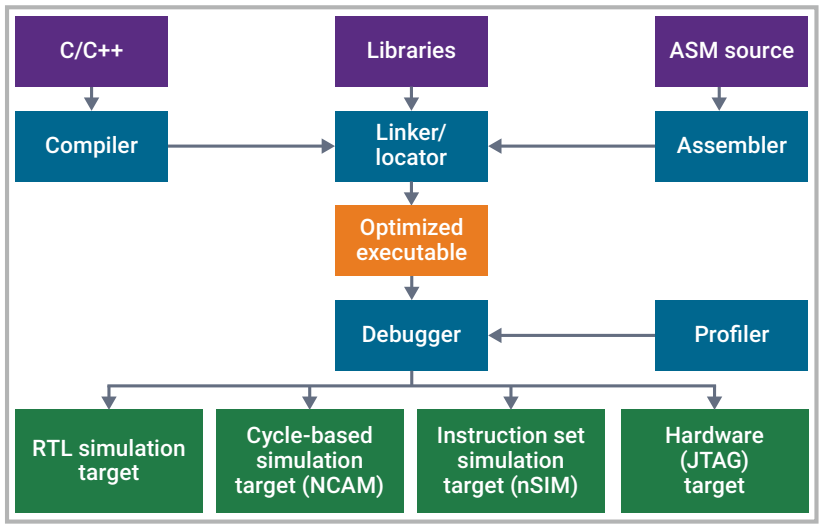

Figure 1: The ARC MetaWare Development Toolkit offers a complete solution to effectively support the development, debugging, and optimization of applications for the ARC and ARC-V processors

Metaware DT Support	ARC EM/HS	ARCVPX	ARC RMX / RHX / RPX	ARC RHX / RPX+ Vector
Compiler				
C/C++Compiler	X	X	X	X
Open CL C Compiler		X		
Debuggers				
MetaWare Debugger, Proprietary Engine	X	X		
MetaWare Debugger, LLDB Engine			X	X
Graphical Development Environments				
MetaWare IDE (Eclipse based)	X	X		
MetaWare Standalone Debugger GUI	X	X	(*)	(*)
Visual Studio Code MetaWare Debugger Plugin			X	X
Compute Libraries				
Scalar DSP Library	X	X	(*)	(*)
Vector DSP Library		X		(*)
Linear Algebra Library		X		(*)
Vision Library		X		(*)
Runtime Libraries				
Standard C/C++ Libraries	X	X	X	X
Accelerator Runtime (SPEED)		X		
Simulators				
nSIM	X	X	X	X
NCAM	X	X	X	(*)
Safety Certified (Included only in the Metaware DT for Safety product)				
C/C++ Compiler - Safety Certification	X	X	(*)	(*)

(*) Roadmap Item

Table 1: ARC MetaWare Development Toolkit Functionality Supported per Processor Family

Develop Code with the ARC MetaWare C/C++ Compiler

- Highly optimized and robust ANSI C99 and C++ compiler. Supports extensive GNU compiler compatibility
- Standard C/C++ library optimized for deeply embedded applications: small and compact, with full C++ language support
- Leverages industry-standard LLVM Compiler Infrastructure
- Seamless integration with open source and Synopsys virtual prototyping and architecture exploration tools
- Includes Standard Template Library
- Includes compute libraries, SPEED runtime and OpenCL C language support
- Minimal footprint, low-profile library for embedded applications (selectable via command line switch)
- Tool Configuration File (TCF) used by all tools to share ARC core configurations with single file
- Compiler tools and libraries extensively tested with multiple validation test suites
- ARC processor mixed 16/32-bit Instruction Set Architecture (ISA) offers industry-leading code density without the need to align instructions or switch modes
- Includes extensive DSP programming support with native fixed-point types, fixed-point API and comprehensive DSP Library of high-level functions
- Support for user-defined, application-specific instructions and extensions, enabled through ARC Processor Extensions (APEX), with zero overhead intrinsics
- Automatic Overlay Manager saves memory size and associated cost by transparently managing loading and removal of overlays into and from main memory without the need for explicit programming (for specific ARC processors only)
- ELF assembler and linker with extensive command language offering full control over code and data placement and section layout

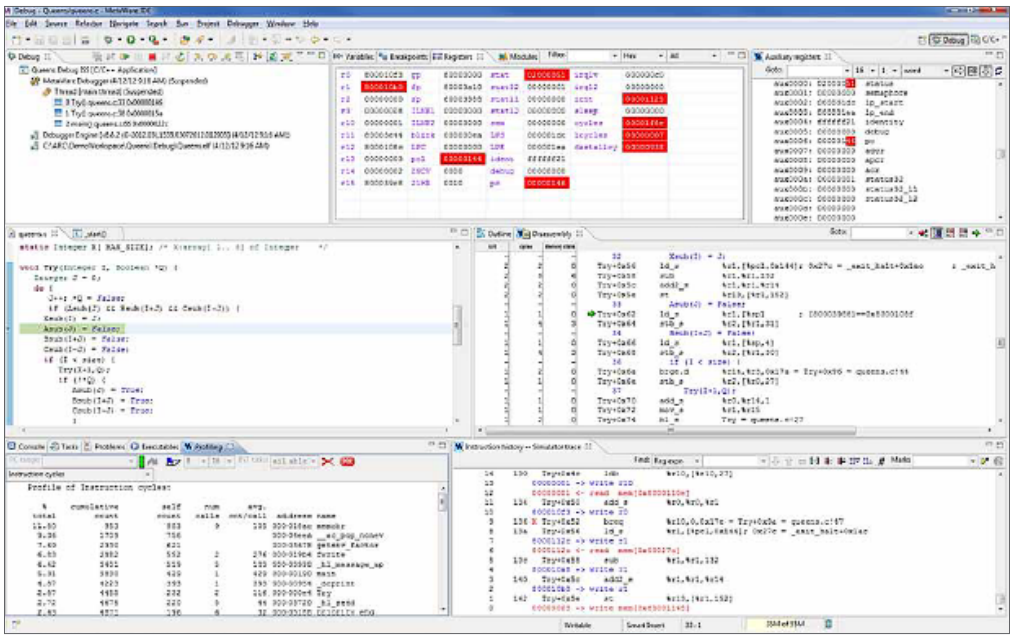

Figure 2: The ARC MetaWare Integrated Development Environment (IDE) gives full debugging and profiling visibility

Debug and Profile Code with the MetaWare C/C++ Debugger

- Both graphical and command-line user interfaces
- Open-interface debugger GUI allows you to design your own plug-ins for adding functionality
- Semantic inspection interface enables you to display your application-specific data in a format that is most useful and meaningful
- OS awareness for the MQX, ThreadX and FreeRTOS RTOSes
- Supports Ashling Microsystems' Opella-XD probes and Digilent JTAG cables
- Supports ARC Real-Time Trace (RTT) with Ashling Microsystems' Ultra-XD trace pod
- Coordinated Multi-Processor Debug (CMPD) controls and coordinates the debugging of multiple processors from a single debug session
- Full support for the complete set of ARC processor configuration options and extensions, including XY-memories and other DSP extensions
- Automatic Overlay Manager awareness (for specific ARC processors only)
- Extensive profiling capabilities that allow you to tune your application and system performance
- Ability to run debugger with hardware as well as simulators using a common user interface regardless of what execution target is used
- Included ARC nSIM Instruction Set Simulator with Near Cycle-Accurate Mode (NCAM), enables application software development and optimization before hardware is available

Manage your Project Through the Modern Developer-friendly ARC MetaWare IDE

- Seamlessly integrate the creation, management and debugging of embedded applications from a single cockpit
- Full integration of the ARC Metaware Compiler and Debugger specific capabilities through a CDT plugin
- Flexibility to incorporate other Eclipse compatible tools from third parties

Linear Algebra, Vector DSP and Vision Libraries

The ARC MetaWare Development Toolkits come with a collection of optimized software compute libraries (Figure 3) including:

- Vector DSP library delivering vector and matrix operations, filters, and orthogonal transform algorithms
- Vector Linear Algebra Library delivering BLAS/LAPACK and supplementary algorithms
- Vision library delivering classic computer vision kernels to accelerate vision algorithms and applications running on the ARC VPX. Kernels include resize, color space conversion, various filters and pixel-wise processing. Kernels can be used standalone, or in conjunction with the NN SDK to do pre- and post-processing of images.

These libraries are implemented using Vector-Length Agnostic C/C++ programming model to ease software portability across configurations of ARC processors, specifically the VPX processors. By using these libraries, customers can simplify application development by relying on pre-verified and fully tuned implementations of mathematical, digital signal processing and linear algebra algorithms covering Radar, LiDAR, Sensor Fusion and many other computational domains.

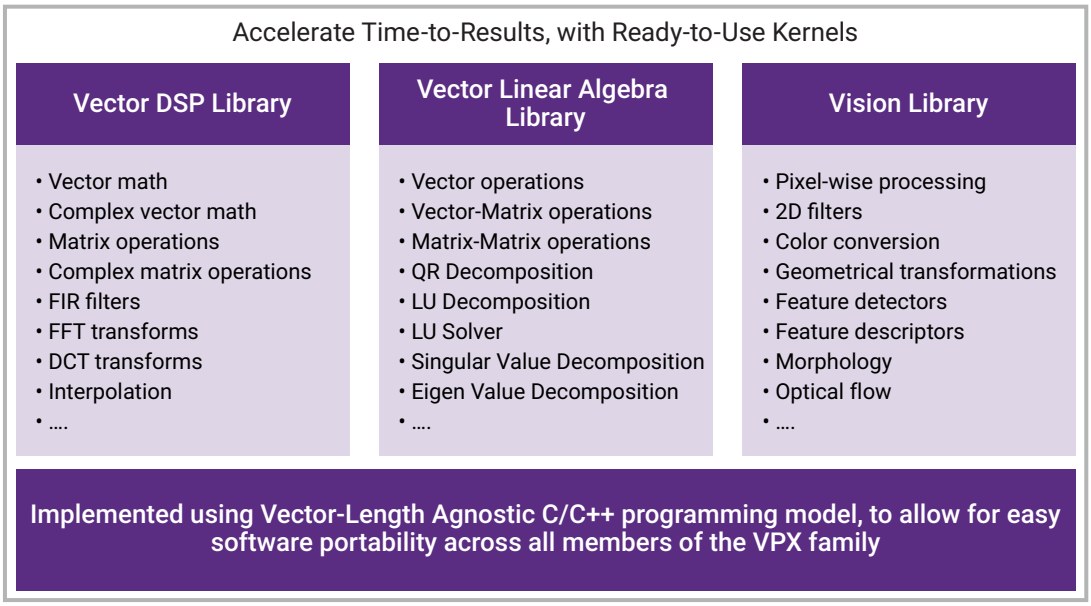

Figure 3: MetaWare Linear Algebra, Vector DSP and Vision Libraries

ARC nSIM instruction Set Simulator with NCAM

The Synopsys ARC nSIM Instruction Set Simulator provides an instruction accurate processor model for the Synopsys ARC processor families. Such processor models take the software development out of your products' critical path by enabling an early start as well as increased efficiency through enhanced visibility and control. The nSIM models provide a complete and accurate hardware/software interface model of the ARC processors that guarantees binary compatibility of product code between the simulation platform and the hardware.

- Single product supporting instruction accurate modelling of Synopsys ARC Classic (ARC HS, ARC EM, ARC 600, ARC 700 and ARC AS200) and ARC-V (ARC RMX, ARC RHX and ARC RPX) families
- Accurate cycle-based (NCAM), interpretive and high-speed JIT-compilation (just-in-time) modelling variants
- Models for APEX processor extensions can be added as an extension DLL or as a separate SystemC component; automatically generated or handcrafted
- OSCI TLM-2.0 SystemC standard interface for SoC level modelling
- Synopsys Virtualizer and Platform Architect integration layers on top of SystemC interface provide access to advanced debugging and profiling capabilities offered by Synopsys SoC prototyping platforms
- Standard gdbserver protocol as well as optimized proprietary API for interfacing with a debugger
- Semi-hosting support with MetaWare Hostlink and standard RISC-V interfaces
- Available for 64-bit Windows and Linux simulation hosts

Simulink Model-Based Design Support

The MetaWare Development Toolkit is compliant with Simulink® Model-Based Design flow. Model-based Design takes advantage of ARC processor Hardware Support Packages. It allows users to develop algorithm at a higher level of abstraction. The Simulink Model-Based Design flow automatically generates Vector DSP Library C code with highly-optimized library function calls to the ARC processor. The Vector DSP Library and Vector Linear Algebra Library are used as code replacement libraries to produce the optimized code that can then be compiled and run on the ARC processor.

MetaWare for Safety (Included in the Metaware Development Toolkit for Safety products)

For developing safety-related software to meet ISO 26262, certified versions of the Metaware Development Toolkit and the MetaWare Compiler are available. These products have been certified by SGS-TÜV Saar GmbH as ASIL-D ready and they include a Safety Guide and Safety Manual for the using the MetaWare tools in such applications.

MetaWare Lite

A code-size restricted version of the MetaWare Development Toolkit is available for free from the Synopsys web site. MetaWare Lite has a number of restrictions, including a code-size limit of 32 Kb.

embARC Open Software Platform

The embARC Open Software Platform (OSP) is a comprehensive suite of free and open-source software, including drivers, operating systems, middleware and utilities, for embedded software development on ARC processors. It is available from embARC.org web site. Both the MetaWare Development Toolkit and MetaWare Lite support software development with embARC OSP.

Deliverables

The Synopsys ARC MetaWare Development Toolkit is delivered as a Windows or Linux installer that installs all tools, libraries and Eclipse CDT plugins, and comes with an extensive set of examples and demos.

Documentation

The following documentation is available for the Synopsys ARC MetaWare Development Toolkit:

- MetaWare Release Notes
- MetaWare Quick Start Guide
- MetaWare IDE User Guide
- MetaWare Getting Started Guide
- MetaWare C/C++ Compiler User Guide
- MetaWare Debugger User Guide
- MetaWare ELF Assembler User Guide
- MetaWare ELF Linker and Utilities User Guide
- MetaWare C/C++ Language Reference Manual
- MetaWare C Library Reference Manual
- MetaWare C++ IO Streams Library Reference Manual
- MetaWare Debugger Extensions Guide
- MetaWare Automated Overlay Manager User Guide
- ARC Fixed-Point Reference Guide
- ARC DSP High-Level Library Databook
- nSIM Release Notes
- nSIM User Guide

About Synopsys IP

Synopsys is a leading provider of high-quality, silicon-proven semiconductor IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, interface IP, security IP, embedded processors, and subsystems. To accelerate IP integration and silicon bring-up, Synopsys' IP Accelerated initiative provides architecture design expertise, hardening, and signal/power integrity analysis. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market.

For more information on Synopsys IP, visit synopsys.com/ip.

SYNOPSYS®

02/04/25.SNPS1575094248-ARC-Metaware-Toolkit-DS.