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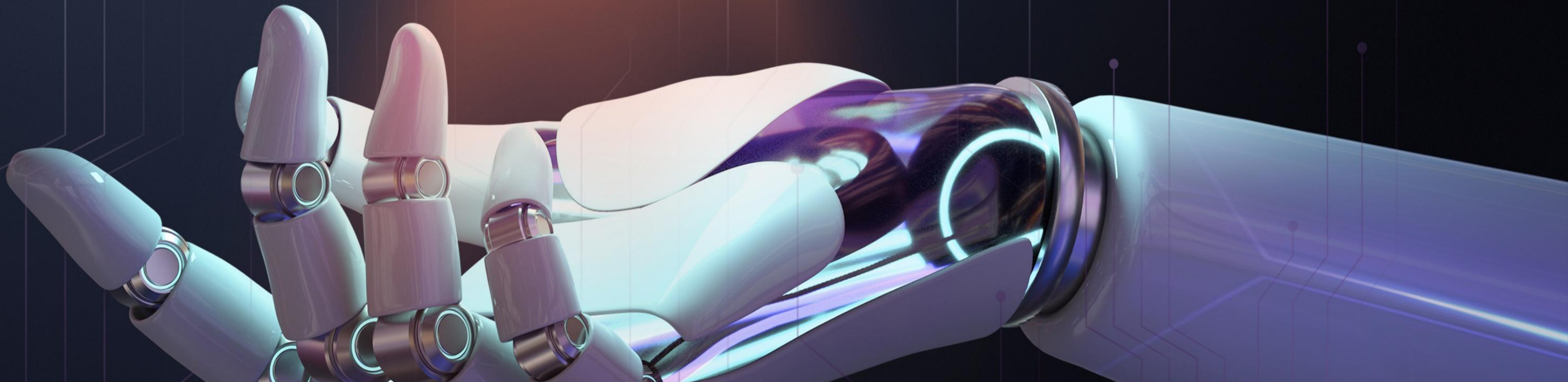
MIPS™

a GlobalFoundries company

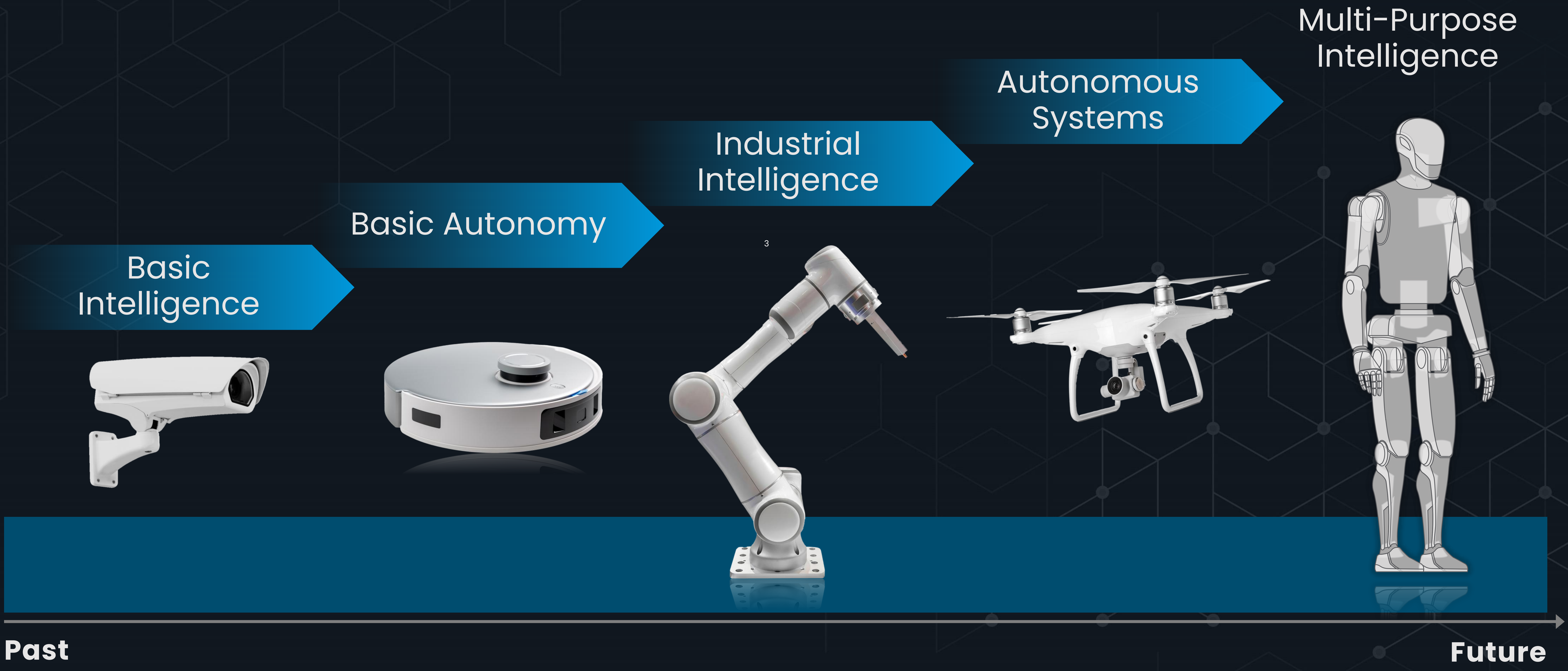
Physical AI Is Built On MIPS

Overview

Jan 14th 2026



AI is Transforming the Physical World



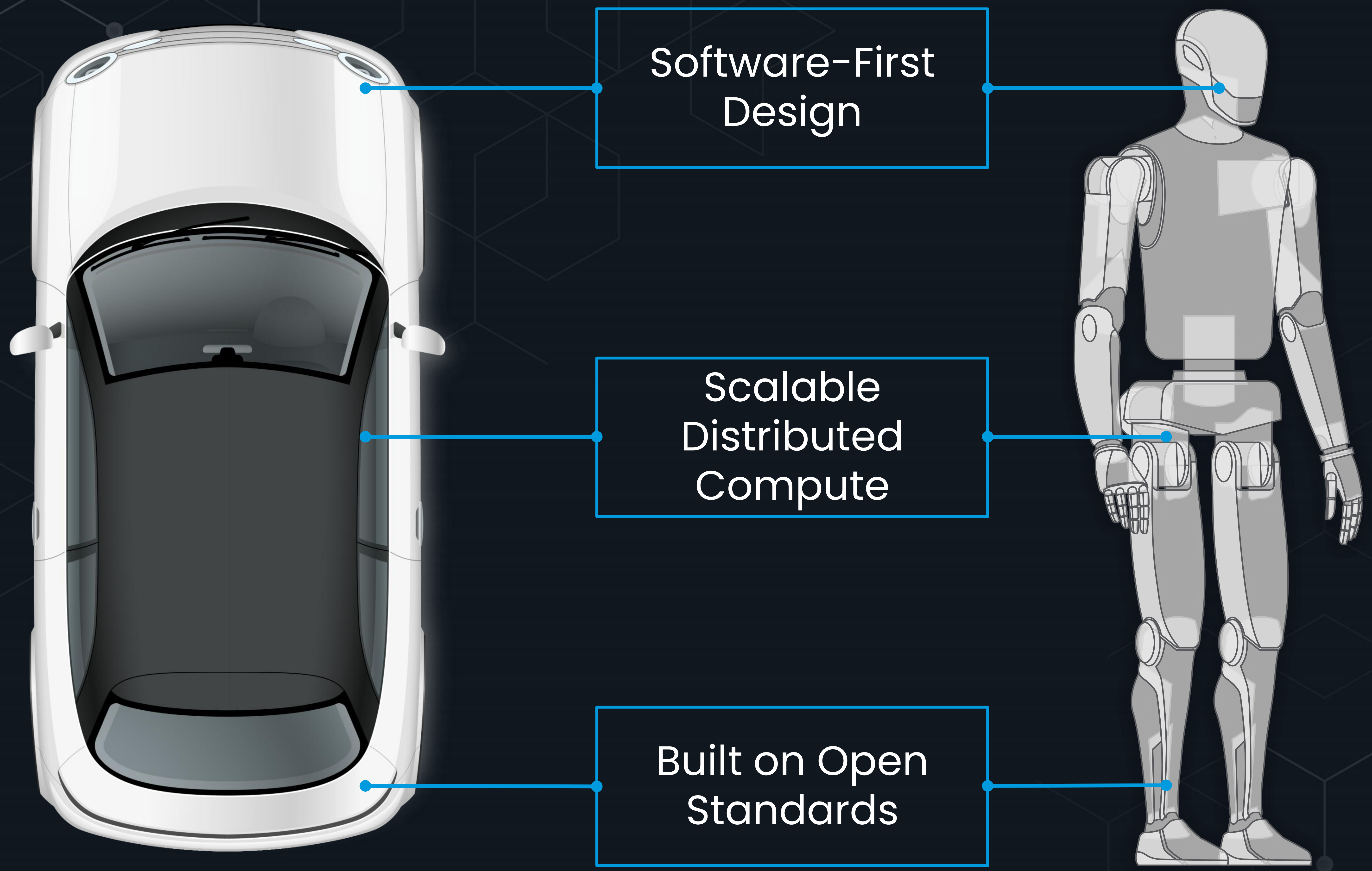
The Compute Challenge of Physical AI

Dynamic, Unpredictable Environments

SENSE | **THINK** | **ACT** | **COMMUNICATE**

Gather Environment Data → Autonomous Decision Making → Movement & Action → Data & Status Updates

The Growth of AI to the Edge Changes Design Approach



Software-Defined Architectures

- Software-First Design
  - Standardized Compute Blocks
  - Application Specific Optimization
- Standards-Based Technology
  - Open, Modular ISA
  - Common code base
  - Shared Toolchain
  - Commercial Vendor Support
- Scalable, Distributed Compute
  - Workload Focused SoCs
  - Software Enhanced Function

Software-First Design: Software & Tools

Evaluate

Workload Modeling with Virtual Core IP

Develop

Software/ Hardware Co-Design

Deploy

Digital Twin Lifecycle Management

Software Guided Intelligence

- Earlier insights for smarter designs
  - Atlas Explorer virtual platform
  - Atlas IP Core Models
- Platform Design Insights
  - Cycle Accurate Modeling
  - AI-Enhanced SW/HW Co-design
- Application Optimization
  - Code Migration & Tuning
  - Workload Focused Toolchains
  - AI-Powered Software Tuning & Optimization

Standards Based Technology: RISC-V Processor IP

Base ISA

Profile Compliant Processor

Application Extensions

Modular ISA Extensions

Workload

Application Specific Instructions

Open, Modular, Extensible

- Standardized Programming Model
  - Easy to Adopt & Use
  - Common Code Bases
  - Commercial & Open-Source Toolchains
- Software Defined Functionality
  - Base Profile Compliant with RISC-V Extensions
  - Application Specific Instructions
  - Workload Tuned Architectures

Scalable Distributed Compute

Scalable Autonomous Edge Architectures

- Reduced use of low-volume, high-cost ASICs in single applications
- Differentiated Product Design
- Re-use platform architectures in adjacent markets
    - Economy of Scale
    - Supply Chain Management
- Reduced Time-to-Market
- Shared Development Costs
- Higher Quality
- Simpler Support

Mapping Physical AI to Compute Engines

Breaking Down the Workload Into Engines

SENSE	THINK	ACT	COMMUNICATE
Multi-stream Data Aggregation & Control	On-Device Transformer & Language Model Inference	Real-Time Control & Low-Latency Event Processing	Low-Latency, High-Throughput, Secure Data Orchestration
Compute-Dense Applications Processor Clusters	Software-First AI Accelerator for Transformer & Language Model Workloads	High-Performance Real-Time Microcontrollers	Multi-Threaded Data Movement Engines
MIPS IP: P8700	S8200	M8500	I8500

MIPS Atlas Portfolio of RISC-V Processor IP

	Transportation	Robotics	Embedded	Technology RISC-V®
M8500 ACT	• Embedded Control Unit • On-board Battery Management • Traction Invertor	• Control Loops • Safety Domain	• Intelligent Power Management • Energy Infrastructure • SSD Channel Controller	**High-Performance 32-bit Microcontroller** • Field-Oriented Control Algorithm Acceleration • Functional Safety (DCLS, ASIL-D, ASIL-B) • Real-Time Multithreading (4-Threads per Core)
I8500 COMMUNICATE	• Zonal Gateway	• Industrial Gateway	• SSD Storage Controller • Communications Infrastructure • Intelligent Networking	**Embedded 64-bit Data Orchestration Processor** • Native Linux/RTOS/Bare metal OS support • 4-Threads per Core, 6-Core Clusters • Scales up to 384 Clusters • Native big-Endian support
P8700 SENSE	• Data Movement Engine (ASIL)	• Data Movement Engine (SIL)	• Data Movement Engine for Smart NIC/DPU • Embedded Applications Processor	**Performance Applications Processor** • 2-Threads per Core • 64-bit Out-of-Order Pipeline • Functional Safety (ASIL-B) • Multicore Cluster scaling
S8200 THINK	• ADAS (Bird's Eye View; OMS/DMS; LKA; Traffic Sign Recognition, etc.)	• Predictive Maintenance • Real-time Monitoring • Vision/Language Models	• On-Device Modern AI Inference	**Embedded Neural Processing Unit** • Support Transformer & Language Models • Area-dense with class-leading TOPS/w • RISC-V Vector & Matrix extension support

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Earlier Insights | Smarter Designs

Software-First Design

Atlas Explorer virtual platform for
Atlas Core Models

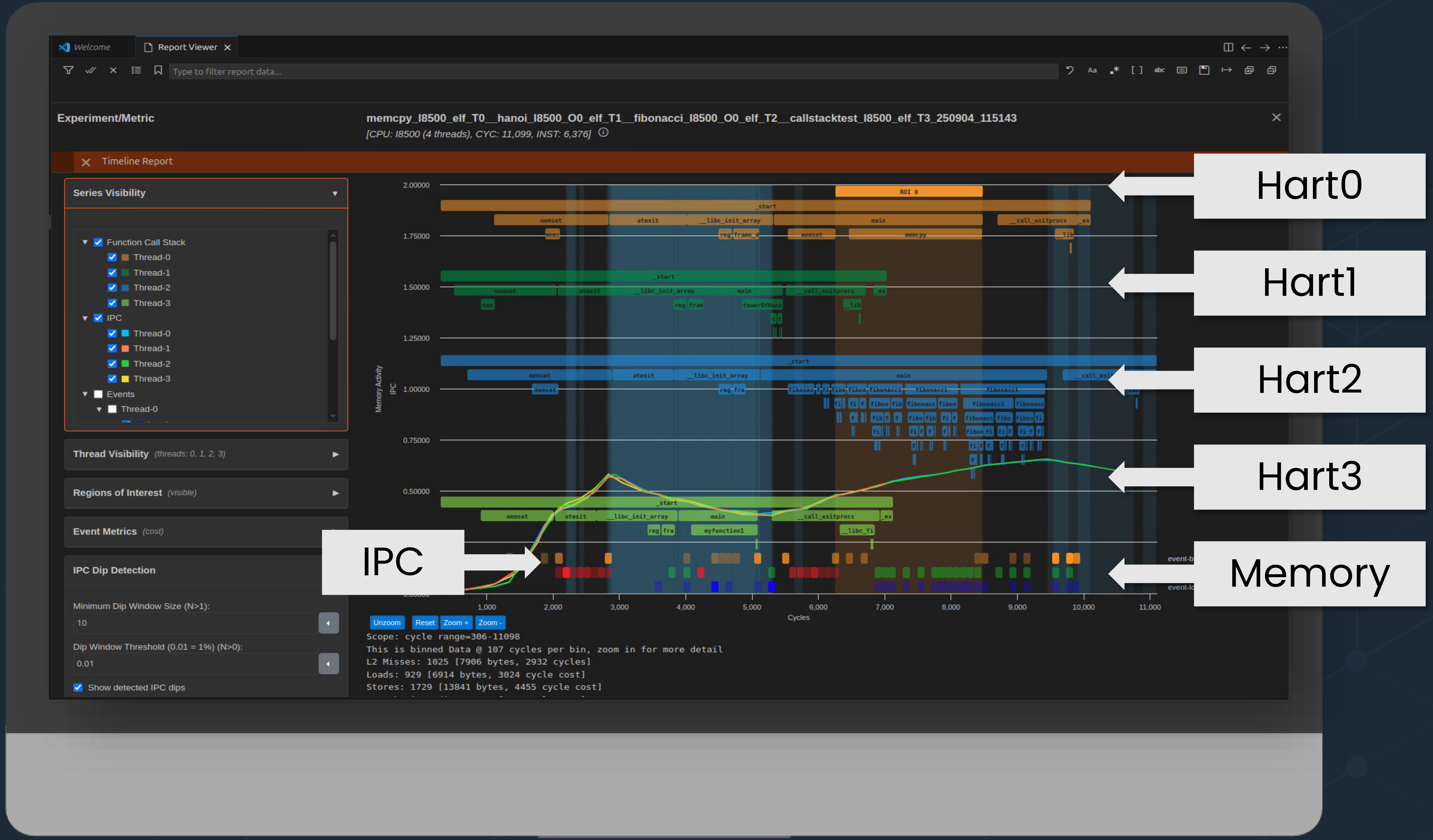
Shift-Left Development

Start your software optimization before
RTL, FPGA, and silicon availability

Platform Design Insights

Branch trends, load/store activity, ALU usage,
register pressure, cache locality, IPC & more

MIPS Atlas Explorer
for Visual Studio Code



MIPS + GF Bring Physical AI to Life

MIPS Workload driven IP & Design

- Software-First Processor IP Design
- Modular Workload Extensions
- Processor IP Optimized for Physical AI
- RISC-V: Open Standard Instruction Set Architecture

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Architecture Influences Technology

Technology Enables Architecture

GF Optimized Process Technologies

- World's most feature-rich FinFET
- FDX: Lowest power, highest integration
- Advanced Packaging: Size, power, performance

Benefits of combined capabilities

Microarchitecture optimizations for efficiency in ultra-low power process technology
Ultra-low power process technology (up to 50% benefit PPA)
Data paths & pipelines to process; Key algorithm acceleration
Industry leading integrated RF & embedded memory (RRAM, MRAM)
Software migration & application development
Dedicated I/O devices enabling dense SoC integration

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Autonomous Edge Applications

Transportation

Automotive Driver Assistance Systems

Self-flying Uncrewed Aircraft

Autonomous Mobile Robot

Robotics

Automated Assembly

Warehouse & Logistics

Humanoid Robot

Embedded

Intelligent Motor Control

Network Data Orchestration

Power Infrastructure

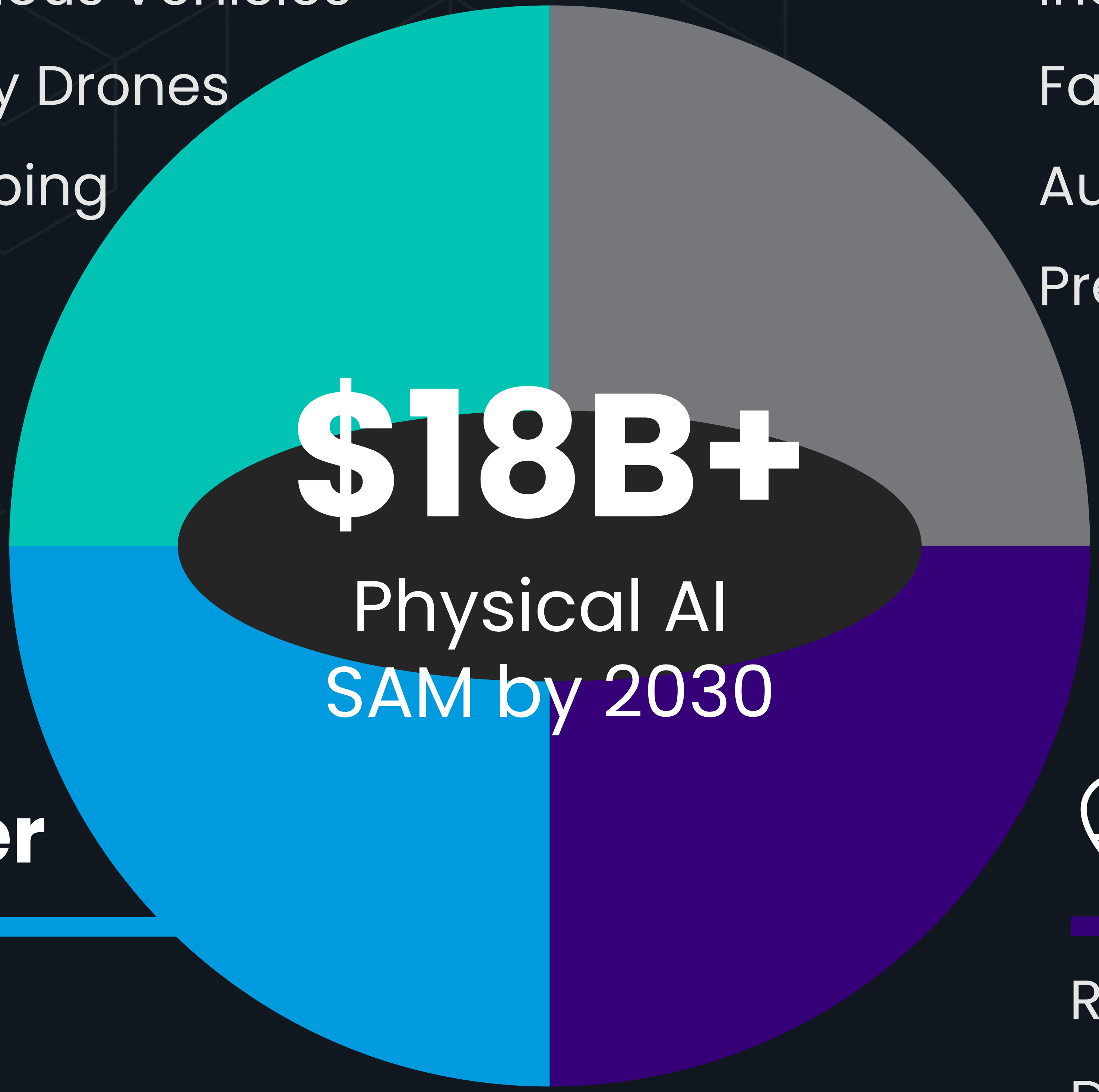
A Significant & Expanded Market Opportunity

Transportation

- Personal Autonomous Vehicles
- Logistics & Delivery Drones
- Autonomous Shipping
- Robotaxis

Industrial

- Industrial Robots
- Factory & Agricultural Cobots
- Autonomous Defense Systems
- Predictive Maintenance Systems



Consumer

- Humanoid Robots
- Smart Glasses
- Smart Home Devices
- AI-Enabled AR/VR

Medical

- Robotic Surgeries
- Diagnostic Wearables
- Medical Smart Sensors
- Smart Drug Delivery Systems

Enhanced Business Model

Differentiated Technology

Custom Silicon

IP Licensing & Royalties

Software

Accretive to GF's Long-Term Goals

SAM based on company estimates

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Thank You

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Endnote

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