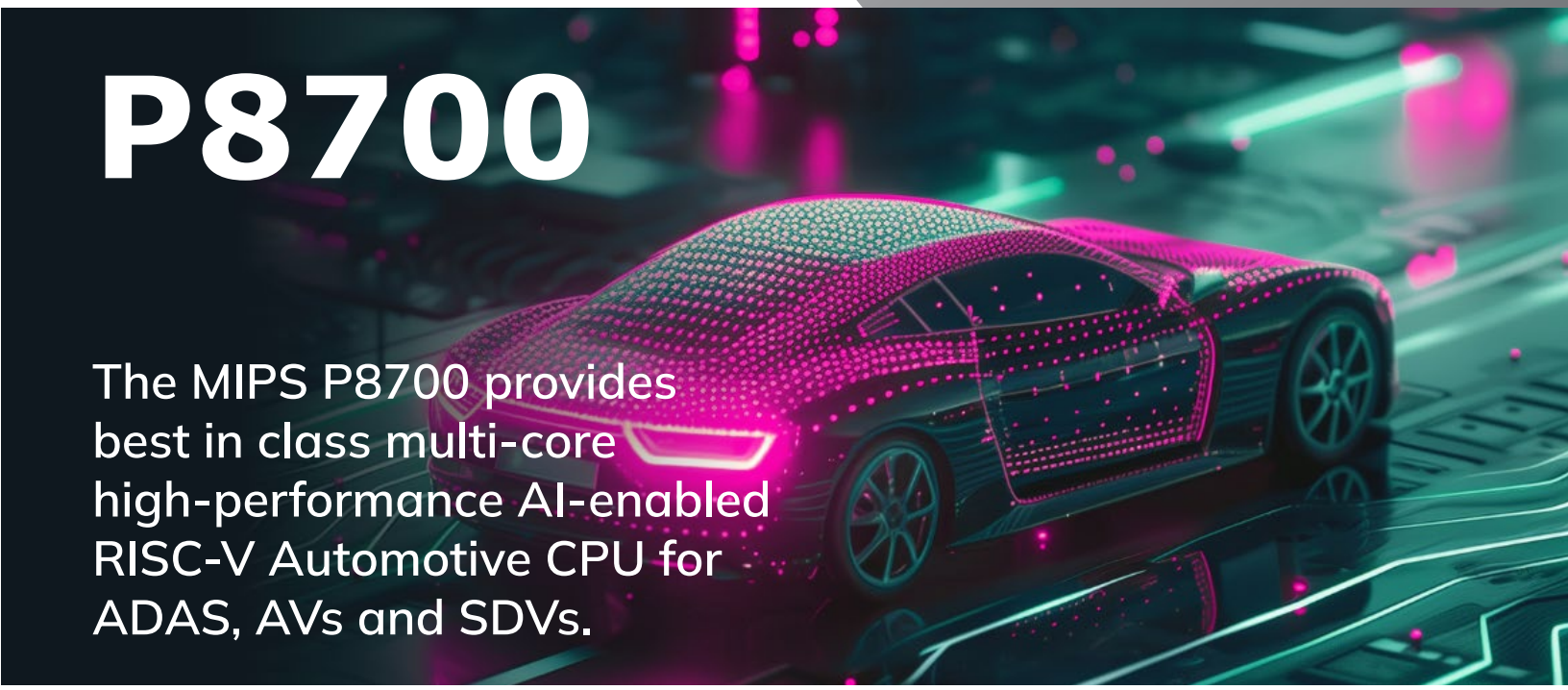
Product Brief

P8700



The MIPS P8700 provides best in class multi-core high-performance AI-enabled RISC-V Automotive CPU for ADAS, AVs and SDVs.

FEATURES

- **High-performance 64-bit RISC-V application processor**
- **2-way simultaneous multi-threading**
- **ASIL-B capable safety element out context**
- **Tightly-coupled accelerator interfaces**
- **Custom built for automotive compute solutions**

ACCELERATING AI

For L2+ ADAS systems with AI autonomous software stack, the MIPS P8700 can offload core processing elements that cannot be easily quantized in deep learning and reduced by sparsity-based convolution processing functions, resulting in more than 30% better AI stack software utilization and efficiency.

The MIPS® P8700 Multiprocessing System is the first RV64GCZba_Zbb compliant CPU IP focused on high performance, data movement and latency-intensive Automotive applications. In addition to implementing the RV64GC RISC-V ISA, the MIPS P8700 also implements proven features from the MIPS ISA, to enhance performance and functionality for automotive and embedded applications.

The MIPS P8700 is built on proven MIPS micro-architecture deployed in more than 28 car models across global OEMs. As such, the P8700 MPS provides best in class multi-core performance for use in system-on-chip (SoC) applications. The P8700 combines a deep pipeline with multi-issue Out-Of Order-execution and multi-threading to deliver outstanding computational throughput.

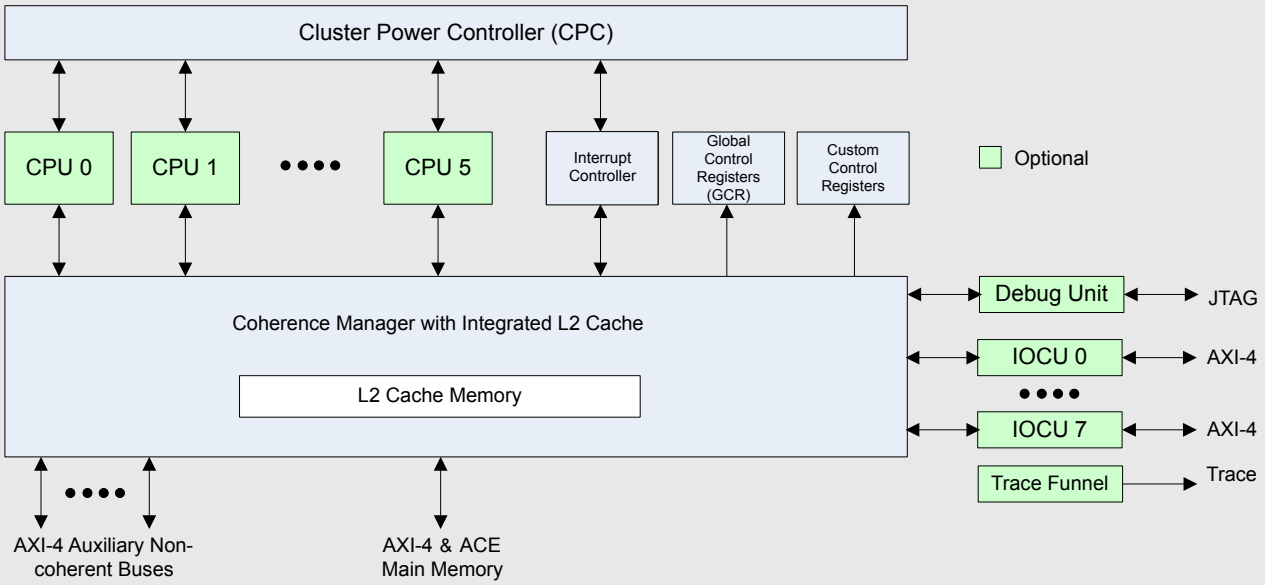


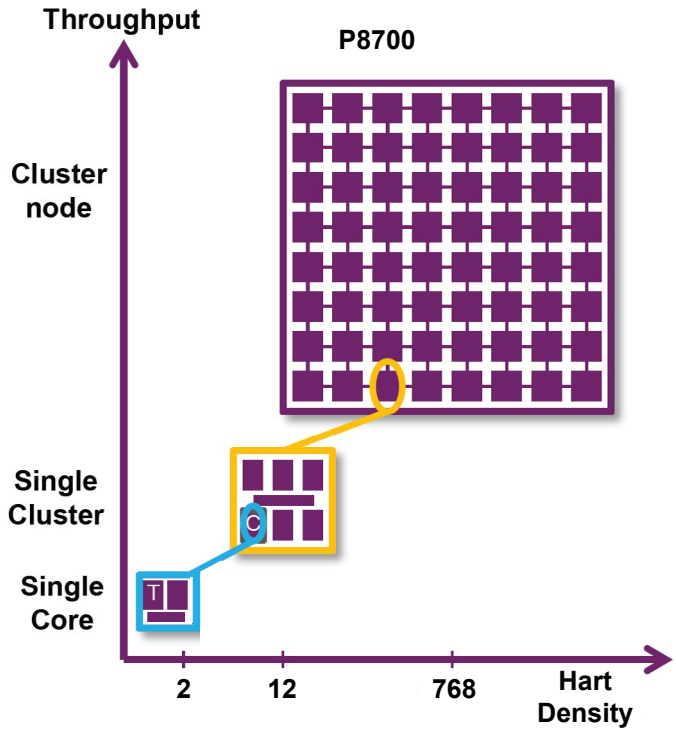
Figure 1. P8700 Multiprocessing System Block Diagram

The P8700 Coherence Manager maintains Level 2 (L2) cache and system level coherency between all cores, main memory, and I/O devices. The P8700 is a configurable and a synthesizable solution. P8700 clusters can be configured with a variable number of cores, I/O coherent interfaces, and L2 cache size. The MIPS P8700 cores can be configured to meet different application requirements with options for Level 1 (L1) cache sizes, and support for 1 or 2 hardware threads.

The MIPS Coherence Manager has an AMBA® ACE interface that enables the P8700 Multiprocessing System to coherently scale up to 64 heterogeneous clusters at the system-on-chip (SoC) level with each cluster supporting of up to 6x P8700 cores each, with up to 2 hardware threads per core.ation with heterogeneous CPU clusters and other accelerators at the system-on-chip (SoC) level.

Each P8700 core implements the RISC-V RV64GC Instruction Set Architecture (ISA) with full hardware multi-threading.

Heterogeneous Inside & Out



- Each CPU in a single cluster can be configured with different combinations of threads and cache sizes.
- IOCU ports enable optimized, low-latency integration of accelerators with shared virtual memory (SVM).
- The latest MIPS Coherence Manager with an AMBA® ACE interface to popular ACE coherent fabric solutions lets designers mix configurations of processing clusters on a chip for high system efficiency.

P8700 Main Components

The P8700 contains the following main components as shown in the block diagram above.

RISC-V RV64GCZba_Zbb CPU Architecture

The CPU architecture (Base ISA and Standard Extensions) supports the instantiation of between 0 and 6 CPU cores, configurable at build time. Each core supports 48-bit virtual and physical addresses, 8-wide instruction fetch, 4-wide decode, 7-wide issue, rename, and graduation. Additional features of the CPU include:

- Out-of-Order Multithreading. Hardware out-of-order multi-threading enables execution of multiple instructions from multiple threads (harts) every clock cycle, providing higher utilization and CPU efficiency.
- P8700 Privileged Architecture. The RISC-V privileged architecture covers all aspects of RISC-V systems beyond the unprivileged ISA, including privileged instructions.
- Functional Safety. The P8700 supports the ASIL-B(D) functional safety standard.

Security and Reliability

The MIPS P8700 implements the RISC-V Physical Memory Protection architecture with 16 regions enabling isolation of critical assets from potential hazards.

Safety

ASIL-B/ISO26262 support with work packages supporting Safety Element Out Of Context (SEOOC) available.

Highest Compute Density

The P8700 implements 2-way symmetric multi-threading enabling it to provide high performance levels with much smaller area.

Ecosystem

P8700 supports RISC-V ISA and has access to the entire RISC-V ecosystem.

I/O Coherence Units (IOCUs)

Hardware I/O coherence is provided by the I/O Coherence Unit (IOCU), which maintains I/O coherence of the caches in all coherent CPUs in the cluster. Up to 8 IOCUs (total number of cores + IOCUs must be no greater than 8).

Cluster Power Controller (CPC)

Individual CPUs within the cluster can have their clock, power, or both gated off when they are not in use. This gating is managed by the Cluster Power Controller (CPC). The CPC handles the power shutdown and ramp-up of all cores in the cluster. The CPC can be controlled via software by accessing and changing values in the registers and by hardware through a signal interface.

Interrupt Controller

The P8700 Interrupt Architecture includes the Advanced Platform-Level Interrupt Controller (APLIC), Advanced Core Local Interrupt (ACLINT) Machine-level Timer, ACLINT Machine-level Software Interrupt (MSWI), ACLINT Supervisor-level Software Interrupt (SSWI) and a Watchdog Timer (WDT). The APLIC Interrupt Controller handles the distribution of interrupts among the CPUs and harts in the cluster.

Global Configuration Registers (GCR)

The Global Configuration Registers (GCR) are a set of memory-mapped registers that are used to configure and control various aspects of the Coherence Manager and the coherence scheme.

Custom GCRs

The Coherence Manager (CM) provides the ability to implement a 64 KB block of custom registers that can be used to control system level functions. These registers are user defined and then instantiated into the design. Two global registers are provided by the CM, the Global Custom Base register, and the Global Custom Status register.

Debug Unit

The Debug Unit (DBU) is an optional component that enables debug using a probe connected through a JTAG scan chain. The DBU contains the single TAP controller in the cluster, which can access registers through the cluster. The DBU also contains a RAM to hold instructions and data accessed by the cores while in debug mode. The Debug port supports multi-core debug via the JTAG interfaces.

Trace Funnel

The P8700 core includes trace support for real-time tracing of instructions, data addresses, data values, and performance counters.

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